Improving Thermal stability of Nickle Silicide by Gemanium Ion Implantation

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***Abstract*—The effect of germanium (Ge) ion implantation on the thermal stability of NiSi/Si structure is studied. Ge implantation before NiSi formation results in a very smooth NiSi/Si interface. Both scanning electron microscope inspection and sheet resistance measurement proof that the sustainable process temperature of NiSi/Si structure can be improved by 50-100ºC with high dosage Ge implantation at suitable energy. Ge implantation after NiSi formation has similar effect. These observations can be explained by the stress balance due to Ge pile-up at the NiSi/Si interface. Shallow n^+/p and p^+/n junctions with high thermal stability were also demonstrated using Ge implantation process.**

I. INTRODUCTION

Metal silicides have been used to improve the integrated circuit performance for more than 20 years. Titanium silicide ($TiSi_2$) is the first successful metal silicide been used. The linewidth effect due to hard phase transformation from C49 to C54 makes $TiSi_2$ to be replaced by cobalt silicide ($CoSi_2$) at 0.18um technology node. However, the high Si volume consumption during $CoSi_2$ formation is not compatible with the ultra-shallow junction requirement after 90nm technology node. NiSi is a desireable contact material to Si because of its low resistivity, limited Si consumption, and low formation temperature. However, the agglomeration or formation of the higher resistivity phase $NiSi_2$ must be avoided for device applications.

Several methods have been proposed to improve the thermal stability of NiSi thin film, for example, fluorine incorporation, nitrogen incorporation, and platinum incorporation [1-5]. Among these methods, Ni(Pt) silicide produces the most promising results. The tradeoff is the higher resistivity due to Pt doping. Besides thermal stability, contact resistance is another big issue. It has been reported that NiSi/SiGe contact exhibits contact resistivity close to $1x10^{-8}$ Ω-cm^2 [6]. Since SiGe source/drain has been used on PMOSFET to provide compressive strain to channel, forming NiSi/SiGe contact is straightforward for PMOSFET. NMOSFET does not have SiGe source/drain structure. Therefore, Ge implantation becomes a possible method to improve the NiSi/Si contact. In this work, we reported the effect of Ge implantation on the thermal stability of NiSi/Si structure and demonstrated high quality NiSi-contacted n^+/p and p^+/n shallow junctions.

II. EXPERIMENTAL PROCEDURE

Both blanket samples and p-n junction samples were fabricated. The starting material was boron-doped (for blanket samples and n^+/p junction samples) and phosphorus-doped (for p^+/n junction samples) 6-in Si wafer with resistivity of 15-25 Ω-cm and 2-4 Ω-cm, respectively. After initial cleaning, a 20 nm thick screen oxide was grown on the blanket samples. Some samples were implanted by Ge^+ at 20KeV to a dose of $5x10^{15}$ cm^{-2} or $1x10^{16}$ cm^{-2}. These samples are classified as GIBS (Ge Implantation Before Silicidation) samples. The project ranges (R_p) of Ge implantation at 20KeV and 50KeV are about 5nm and 25nm below Si surface as simulated by Monte Carlo method, respectively. For the 20KeV samples, Ge implanted layer would be fully consumed during NiSi formation. After removing the screen oxide layer, 25nm thick Ni film was deposited in a physical vapor deposition (PVD) system. A 2-step silicidation process was employed to form silicide [7]. Ge implantation was performed on those samples had not been implanted by Ge before silicidation. The implantation energy was 40KeV so that the R_p is about 17nm below the NiSi surface and all of the Ge ions were located in the NiSi layer. These samples were classified as GIAS (Ge Implantation After Silicidation) samples. Samples were then cut into smaller pieces and received rapid thermal annealing in N_2 ambient at different temperatures for different annealing times. Table-1 lists the process conditions of the blanket samples.

Table-1 Process conditions of the blanket samples.

Category	Energy (KeV)	Dose (cm^{-2})	Annealing Temperature (ºC)	Annealing Time (sec)
GIBS	50, 20	$5x10^{15}$	500, 600, 700, 750, 800, 850	10, 30, 60
GIAS	40	$1x10^{16}$		

Table-2 Process conditions of the pn junction samples.

Category	Species	Energy (KeV)	Dose (cm^{-2})	Annealing Temperature (ºC)
p^+/n	Ge, BF_2	Ge:30 BF_2:20	Ge:$1x10^{16}$ BF_2:$5x10^{15}$	500, 550, 600, 650, 700
n^+/p	Ge, P	Ge:30 As:35	Ge:$1x10^{16}$ As:$5x10^{15}$	

Typical LOCOS isolation was employed to fabricate pn junctions. Only GIBS junction samples were fabricated. Because no screen oxide was grown before ion implantation, the Ge implantation energy was reduced to 30KeV to obtain a similar R_p of about 30nm below Si surface, which is similar to the R_p of Ge implantation at 50KeV through a 20nm thick screen oxide. To form n^+/p and p^+/n junctions, As^+ and BF_2^+ ions were implanted at 35KeV and 20KeV, respectively, to a dose of $5x10^{15}$ cm^{-2}. A spike annealing to 1025ºC was performed to activate the dopants. The silicidation process was identical to that used to fabricate blanket samples. Table-2 lists the process conditions of the pn junction samples.

Sheet resistance (R_s) of NiSi film was measured by a four-point probe method. Surface morphology was inspected by scanning electron microscope (SEM). Cross-sectional structure was inspected by transmission electron microscope (TEM). Phases were identified by X-ray diffraction (XRD). Depth profiles of species were analyzed by Secondary Ion Mass Spectroscope (SIMS). Current-voltage (I-V) characteristics of junctions were measured by a semiconductor parameter analyzer of model Agilent 4156C.

III. Results and Discussions

A. Sheet Resistance

Fig.1 shows the R_s as a function of annealing temperature of the GIBS samples. The annealing time is 10 sec. Higher Ge implantation energy results in better thermal stability. Higher implantation dose also results in better thermal stability. The R_s of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2} does not degrade after annealing at 850ºC for 10 sec. The GIAS samples exhibit the same trend that higher Ge dose results in better thermal stability as shown in Fig.2.

Fig.3 shows the effect of annealing time of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2}. As the annealing time extends to 30 sec or longer, the sustainable temperature reduced 50 ºC, i.e. from 850 ºC to 800ºC. Similar result of the 50 ºC reduction of sustainable temperature is observed on the other samples, including the GIAS samples. The thermal stability of 30 sec annealed samples and 60 sec annealed samples are similar.

B. Micro-Structure Analysis

Fig.4(a)-(d) show the surface morphology of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2} after annealing at different temperatures. Agglomeration phenomenon is observed on the 800 ºC annealed sample. The 750 ºC annealed sample exhibits a very smooth NiSi surface. The inset in Fig.4(b) show that the 700ºC annealed sample without Ge implantation has agglomerated.

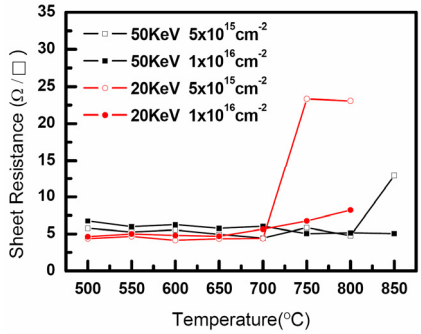

Fig.1 Sheet resistance of the GIBS samples after rapid thermal annealing for 10 sec.

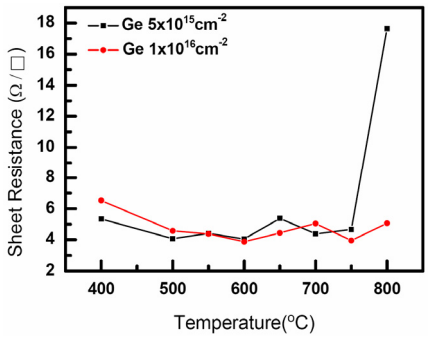

Fig.2 Sheet resistance of the GIAS samples after rapid thermal annealing for 10 sec.

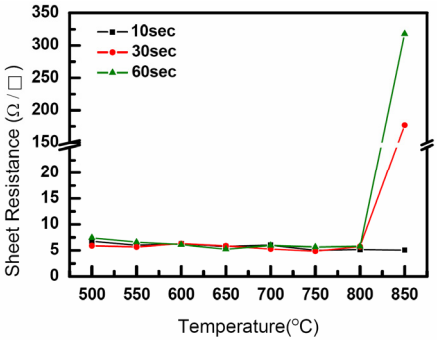

Fig.3 Sheet resistance of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2} after rapid thermal annealing for different times.

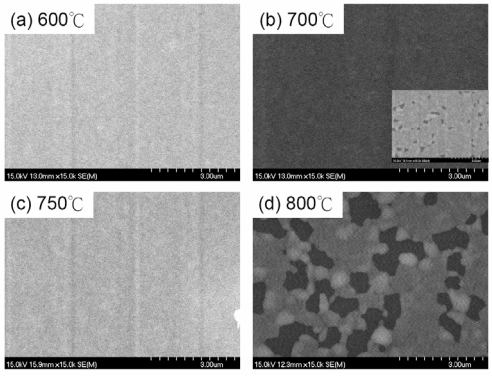

Fig.4 Surface morphologies of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2} after annealing at (a) 600ºC, (b) 700ºC, (c) 750ºC, and (d) 800ºC. The inset in (b) is the sample without Ge implantation after 700ºC annealing..

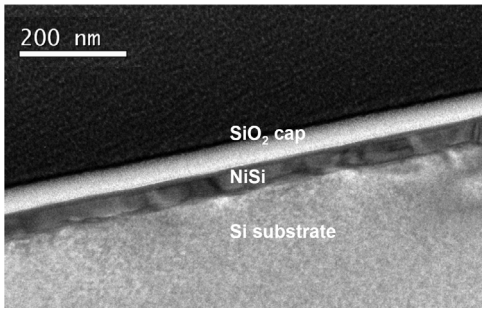

Fig.5 Cross-sectional TEM micrograph of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2} after annealing at 750ºC for 30 sec.

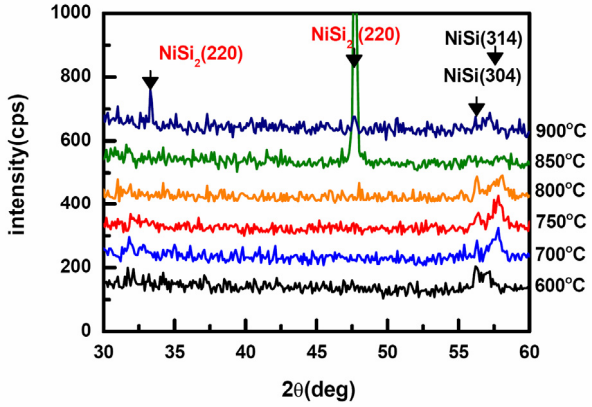

Fig. 6 XRD spectra of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2} after annealing at different temperature for 30 sec.

Fig.5 shows the cross-sectional TEM micrograph of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2} after annealing at 750ºC for 30 sec. The NiSi thickness is 45nm, which translates to a resistivity of 21 μΩ-cm. This value is slightly higher than the bulk value but is much lower than the resistivity of NiSiGe and Ni(Pt)Si [8-10]. No Ge implantation induced crystal defects are observed. The NiSi/Si interface is very smooth even after a 750ºC annealing and could be attributed to the effect of Ge pre-amorphorization.

C. Phase Indetification

Fig.6 shows the XRD spectra of the GIBS samples with Ge implantation at 50KeV to a dose of $1x10^{16}$ cm^{-2} after annealing at different temperatures for 30 sec. The NiSi phase remains stable up to 800 ºC even if agglomeration has occurred at this temperature. The $NiSi_2$ phase occurs at 850ºC. This result indicates that the existence of Ge can retard the phase transformation from NiSi to $NiSi_2$ and phase transformation lags behind agglomeration.

D. Depth Profile Analysis

Fig.7 and 8 show the depth profiles of the p^+/n and n^+/p junction samples after annealing at 600ºC for 30 sec. Most Ge atoms pile up at the NiSi/Si interface. This high concentration Ge layer may relax the interface stress and then improves the thermal stability. Only few Ge atoms incorporate into NiSi layer so that the resistivity of the NiSi layer is low enough as presented in section III-B.

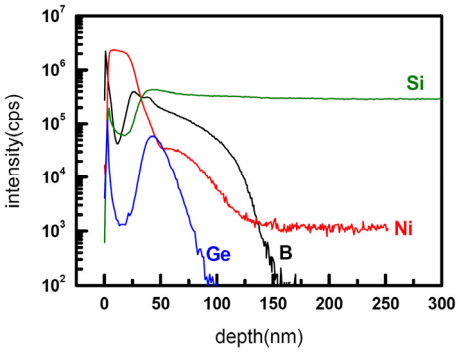

Fig.7 SIMS depth profile of B, Ni, Si, and Ge of he p^+/n junction after annealing at 600ºC for 30 sec.

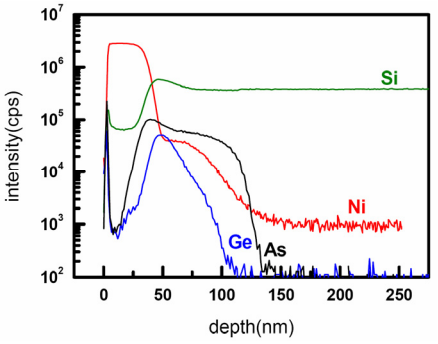

Fig.8 SIMS depth profile of As, Ni, Si, and Ge of he n^+/p junction after annealing at 600ºC for 30 sec.

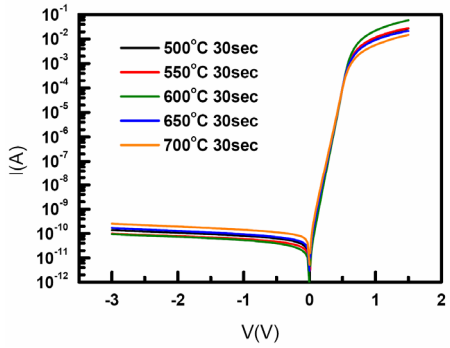

Fig.9 Typical I-V characteristics of the p^+/n junctions after annealing at different temperatures.

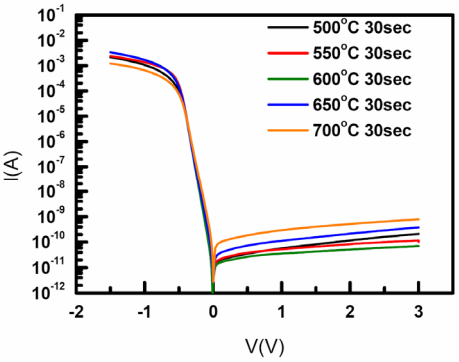

Fig.10 Typical I-V characteristics of the n^+/p junctions after annealing at different temperatures.

The junction depths of p^+/n and n^+/p junctions are about 0.12μm and 0.09μm beneath the NiSi/Si interface obtained by SIMS analysis. The forward current has an ideality factor of around 1.1. The leakage current slightly decreases as the annealing temperature increases from 500 ºC to 600 ºC and then slightly increases as the temperature increases further. Because all samples had been annealed at 1025 ºC before silicidation, the reason for leakage current reduction is not clear at this moment. It might be owing to the annihilation of the PVD induced defects. The leakage current increase at temperatures higher than 600 ºC may be due to the Ni dissolution and diffusion toward the metallurgic junction. The leakage current densities of the Ge implanted sample are similar to those of the samples without Ge implantation (not shown). As shown in the inset of Fig.4(b), the NiSi film without Ge implantation agglomerates at 700 ºC. The similar leakage current behavior should be because the junction is not shallow enough.

IV. CONCLUSIONS

The effect of Ge implantation on the thermal stability of NiSi/Si is studied. Ge implantation before NiSi formation results in a very smooth NiSi/Si interface. The sustainable process temperature of NiSi/Si structure can be improved by 50-100ºC with high dosage Ge implantation at suitable energy. Ge implantation after NiSi formation has similar effect. These observations can be explained by the stress balance due to Ge pile-up at the the NiSi/Si interface. Because only few Ge atoms remain in NiSi layer, the resistivity is close to the bulk value. The phase transformation from NiSi to $NiSi_2$ is retarded to 800 ºC due to the existence of Ge. Shallow p^+/n and n^+/p junctions with high thermal stability were also demonstrated using the Ge implantation process. These results suggest that the Ge implantation is a promising technique for ultra shallow junction applications.

ACKNOWLEDGMENT

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