



A Cooperation Agreement for a Small Versatile 10 Gigabit Transceiver Package

Issue 2.0b

7th April 2005

1. Revision

Revision	Date	Author	Purpose/Changes
0.9	31 st July 2002	Kim Leeson Keith Everett Antony Spilman	First Public issue
1.0	30 th Jan 2003	Kim Leeson Lars Lindberg Jerry Malagrino Ed Bright Antony Spilman	First ratified revision
1.0b	28 th Feb 2003	Antony Spilman	See below
2.0	11 th Jan 2005	Michael Lawton Kim Leeson	Public version 2.0
2.0b	7 th April 2005	Ed Bright Jerry Malagrino Craig Hunter Kim Leeson	Changes to incorporate definitions that prevent damage to the linecard if a module is accidentally inserted upside down.

Revisions between 1.0 and 1.0b

Page 10: Added Multiplex and Triquint contact info.

Page 11: changed Pin #38 and #68 to short pins per XENPAK MSA

Page 13: Added Detail 1 to make design of module rear section more understandable.

Page 13: Clarified dimension of transceiver slot as 0.87+/-0.13.

Page 13: Clarified dimension from datum B to rear edge of Bezel and Datum B front edge of snout (16.7 and 30.5 respectively) as reference dimensions.

Page 13: Clarified dimension from rear edge of Bezel to end of EMI contact area (4.0) as reference dimension.

Page 13: Added Data F to drawing to clarify NOMINAL position of face plate relative to module.

Page 16: Reformatted 4.1 dimensions on connector pads to be consistent with other annotations

Page 16: Corrected locations of PCB holes for rail from 12.0, 24.0, 36.0, 48.0, 60.0 to correct values of 12.85, 24.85, 36.85, 48.85 and 60.85 respectively.

Page 17: Converted to a landscape layout to enhance readability.

Revisions between 1.0b and 2.0

Page 3: Update Members and representatives

Page 23: Maximum insertion loss increased from 50N to 80N

Pages 11-19: Updates to drawings to reflect

- i) Additional tolerances on electrical connector and pcb land pattern to fix Xenpak shorting issue
- ii) Relaxed tolerances for the placement of the electrical connector with respect to the front panel location
- iii) Definition of two EMI solutions consisting of either compression or perimeter style gaskets.

Page 24: Added additional power classes above the 4W maximum:-

- i) Class I = 4W
- ii) Class II = 4-5W
- iii) Class III >5W

Page 28: Added Xenpak Errata section

Revisions between 2.0 and 2.0b

P6: Added description of latch return – Forced spring latch return is optional.

P6: Redrawn Fig. 1 and Fig. 2. The back of the module now shows a mandatory max 0.3mm radius.

P9: Redrawn Fig. 5 with optional roll pin.

P10: Redrawn Fig. 8 with optional roll pin.

P14: Revised mandatory definition of back of module – squared edge, max 0.3mm radius.

P14: Revised mandatory definition of the back of LOPAK module to ensure relief for a minimum length of 4mm and height from datum E of 2.65mm. This guarantees no shorting to the 70 pin electrical connector if LOPAK is inserted upside down.

P17: Inclusion of 2 optional holes for standard roll pin (1.5mm) to increase rigidity of rails if needed to prevent accidental insertion of MIDPAK upside down.

P20: Redrawn back of module (showing mandatory max 0.3mm radius).

P21: Redrawn back of MID/HI PAK modules (showing mandatory max 0.3mm radius) plus optional roll pin.

P22,23: Redrawn back of example LOPAK with cut out at rear of module.

P24: New statements in 6.18 Mechanical Forces :-

- i) Added Maximum forces relate to insertion of module in correct intended orientation.
- ii) Added Minimum force to insert module incorrectly (upside down) must be >100N
- iii) Added Rail extraction force per pin must be >14.3N per pin.



2. Summary of MSA Group Members

Company	Representative	Contact Details
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3. Table of Contents

1. Revision	1
2. Summary of MSA Group Members.....	5
3. Table of Contents.....	6
4. Purpose and Scope of the X2 MSA	6
5. Operating Guidelines of the X2 MSA	8
6. X2 MSA Mechanical	8
7. X2 Electrical Interface	30
8. Thermal Verification.....	30
9. Xenpak Errata	30

4. Purpose and Scope of the X2 MSA

This Multi-Source Agreement (MSA) defines X2, a compact 10 Gigabit/s optical transceiver. The MSA should be regarded as a supplement to the XENPAK MSA and does not attempt to re-specify areas already covered by XENPAK. Every attempt has been made to make this document succinct and contain only information required to make or use the module.

The X2 MSA specifies a module that is physically shorter than XENPAK, mounts on the topside of the host PCB and uses the established electrical I/O specification



defined by the XENPAK MSA. X2 is initially focused on "second generation" 10 Gb/sec enterprise, storage and telecom applications that do not require the thermal capacity provided by XENPAK.

The X2 platform is designed to use a side rail support system that allows the heat sink and front bezel to be easily adapted to the different needs of the key 10 Gb/sec markets. The structure of the X2 rail system has been carefully designed to allow unblocked airflow over the full length of the top surface area, irrespective of direction. X2 can be mounted on the front panel, mid board, or on a "conventional" PCI or compact PCI "blade". The ability to support different height variants, without changing the side rail support, is also a key X2 strength.

Optically, the X2 MSA supports 802.3ae 10 Gb/sec Ethernet, ANSI/ITUT OC192/STM-64 SONET/SDH interfaces, ITUT G.709, OIF OC192 VSR, INCITS/ANSI 10GFC (10 Gigabit Fibre Channel) and others. X2 is ideally suited for Ethernet, Fibre Channel and telecom switches and standard PCI (peripheral component interconnect) based server and storage connections, where a "half size" XENPAK optical transceiver is desired.

X2 uses the same 70-pin electrical connector as XENPAK and supports implementations of XENPAK's four lane XAUI (10 Gigabit attachment unit interface) at both Ethernet (3.125 Gb/sec) and/or Fiber Channel (3.1875 Gb/sec) rates. X2 will also support the OIF SFI4 P2 and serial electrical interfaces as they may emerge in XENPAK, as well as ongoing maintenance.

Thermal analysis indicates that X2 will support both PCI and transverse applications with an acceptable operating margin. Additionally, the rail system allows for flexibility in heat sink configurations and provides the maximum surface area for cooling. Thermal cooling features can be designed to best meet a particular environment's requirements without alterations to the EMI containment or mounting systems.

5. Operating Guidelines of the X2 MSA

This MSA is bound by the operating guidelines published at:
[http://www.X2msa.org/X2 MSA LEGAL r1a.Pdf](http://www.X2msa.org/X2%20MSA%20LEGAL%20r1a.Pdf)

6. X2 MSA Mechanical

6.1 Introduction to X2 Mechanical Design

This MSA is structured to define a versatile optical transceiver module whose heat-sinks, bezels and EMI/gasket solutions can be easily adapted to different application needs

Configurations for each application are known in this MSA as "personalities" of X2, for example X2 PCI application has a PCI personality. Personalities may differ in areas such as bezel, heatsink and/or gasketing system.



The system constraints that exist for a given application are known as an environment. An environment includes such factors as Metal work and airflow details.

The PCB layout and rail system for X2 are shared for all personalities and environments.

The following sections detail:-

- The X2 personalities and environment for key PCI, front panel and mid board mounted applications.
- The X2 base rail and clip on top shield.
- The PCB layout required for an X2 module and rail.
- PCI, Switch and other environments addressed by an X2 transceiver.

The drawings in this MSA are drafted to conform to ASME Y14.5 -1994.

6.2 Description of Latch System

The X2 MSA specifies a sleeve style latch system. This provides a robust solution to overcome the forces incurred by the 70 pin electrical connector during extraction. The MSA specifies common grip points for the user. Also specified is a standardized retention feature on the rail system for the module to engage into upon insertion.

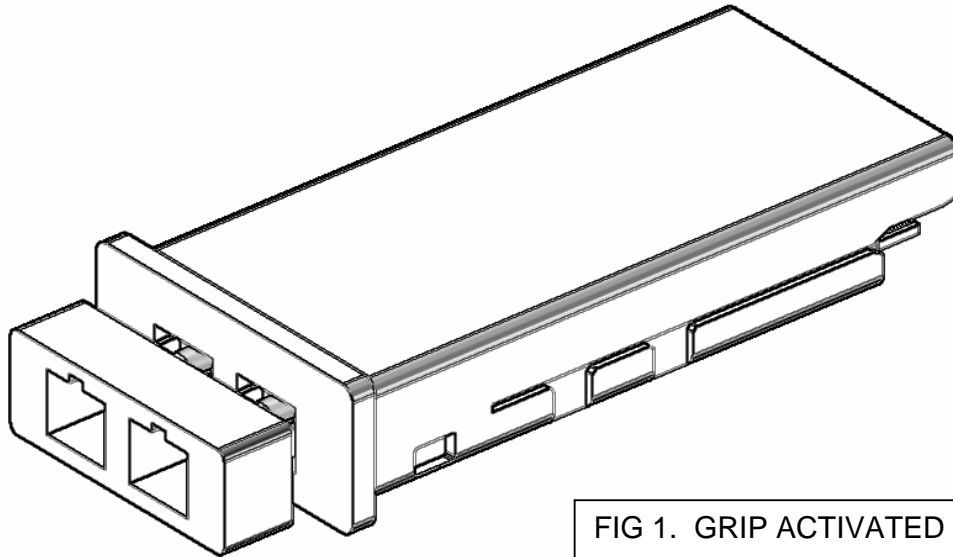


FIG 1. GRIP ACTIVATED

NOTE: FORCED SPRING RETURN ON THIS LATCH IS OPTIONAL

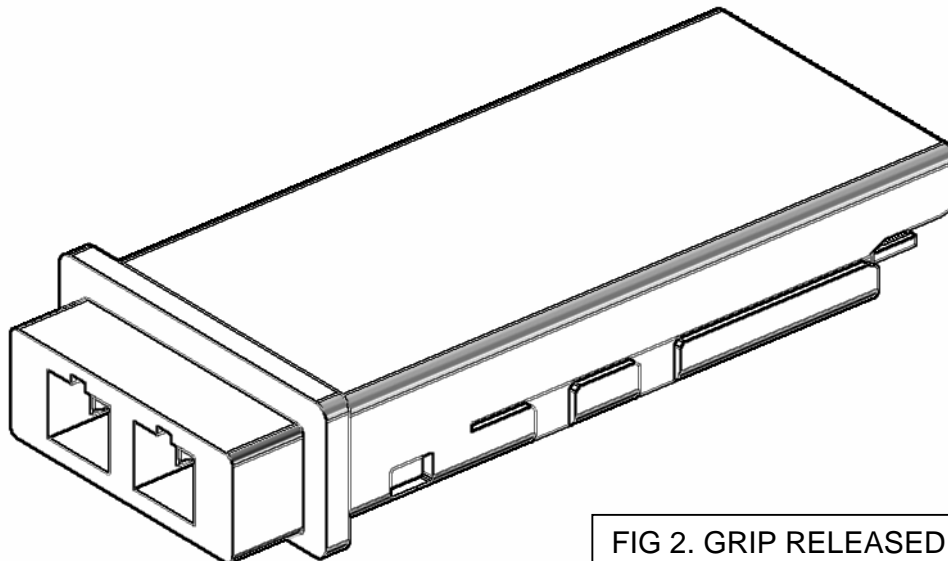


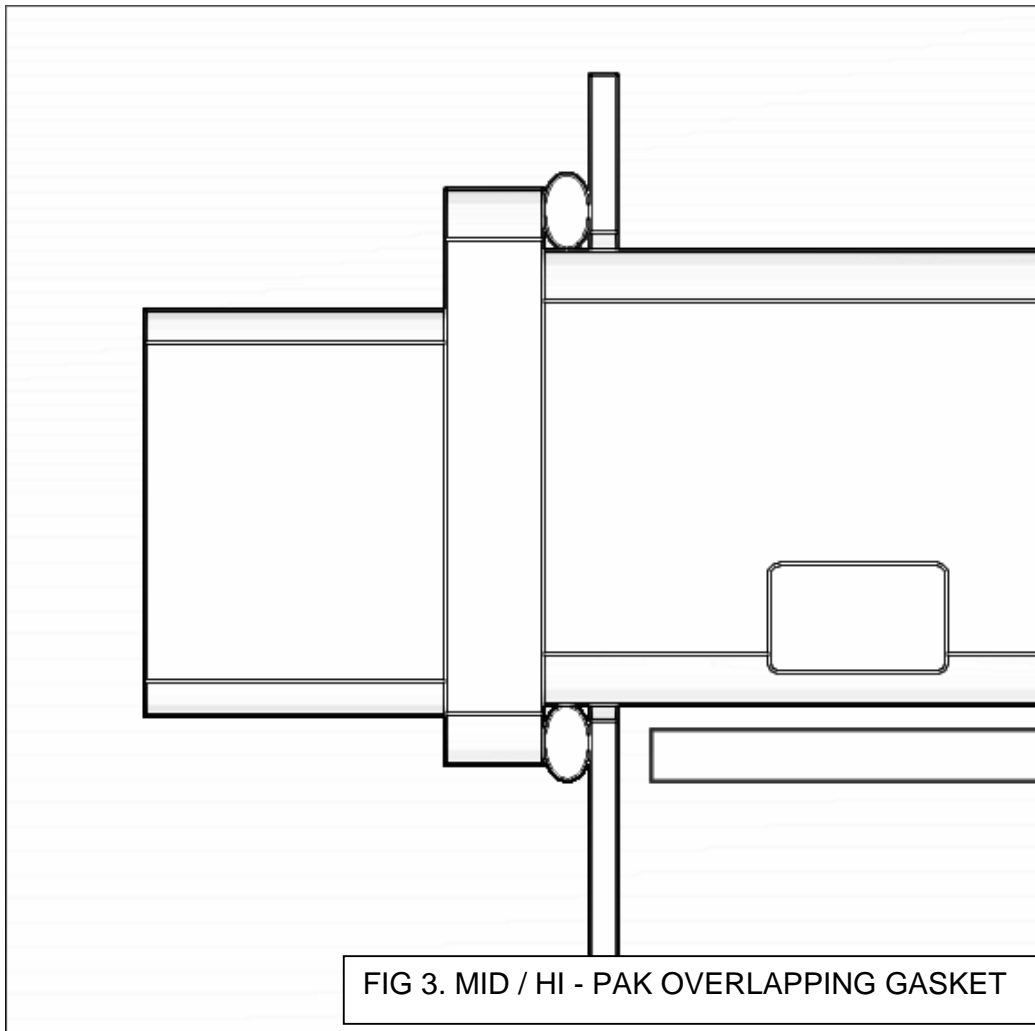
FIG 2. GRIP RELEASED

6.3 Description of the Gasket System

The X2 MSA defines two gasket approaches:-

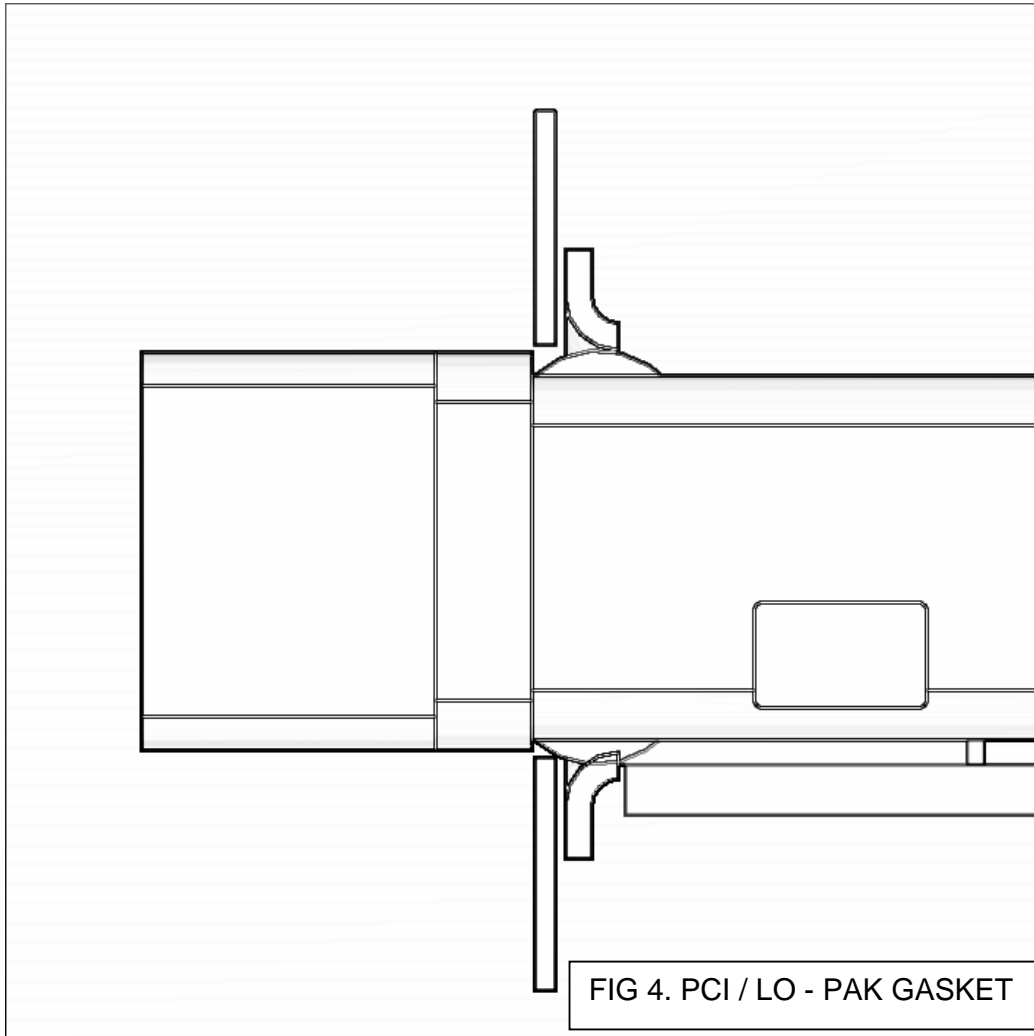
6.3.1 Overlapping Gasket System

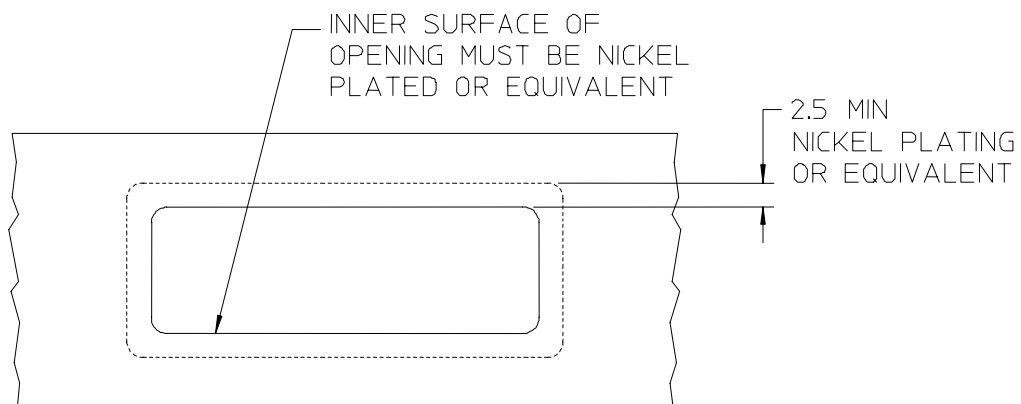
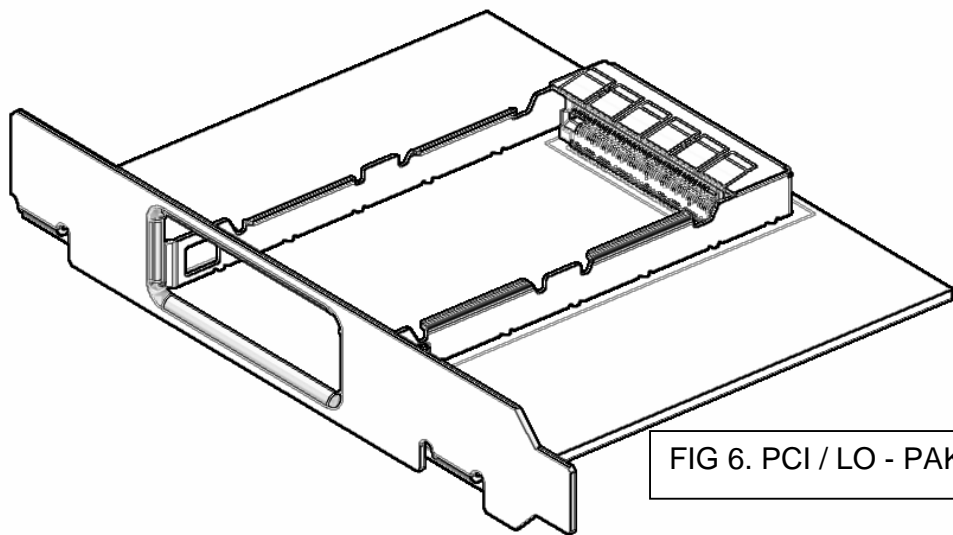
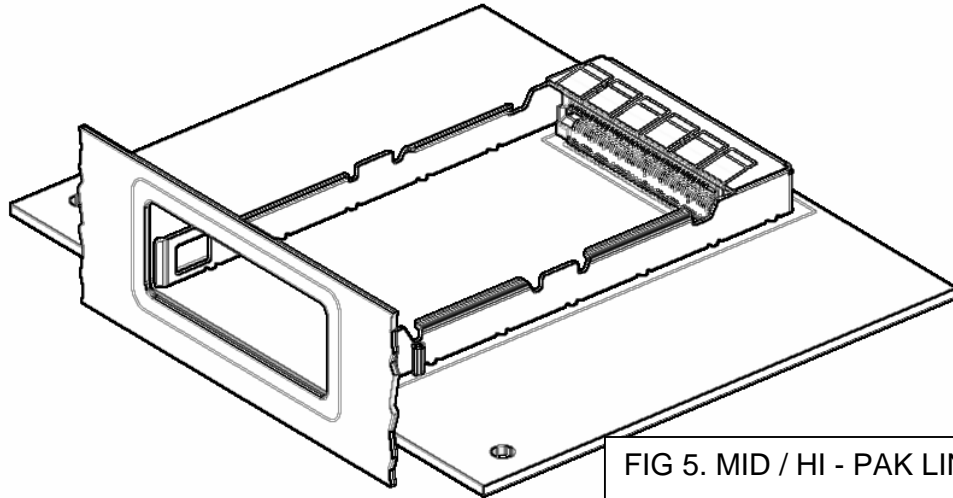
The first provides a bezel that fully overlaps the metal front panel. A compliant gasket is sandwiched between the bezel and the front panel to create a solid EMI solution for all scenarios allowed by the X2 mechanical tolerance stack up. This solution is suitable for highdensity applications such as Ethernet switches.



6.3.2 PCI Gasket System

The second EMI solution has been developed for traditional PCI and uses a bevelled face-plate and spring finger or compressible gasket. Such a system gives a robust EMI solution for applications that have restricted face plate area for all scenarios allowed by the X2 mechanical tolerance stack up.





6.4 Description of the X2 rail system

This MSA contains line drawings of a two-piece rail and top-shield design for X2, however a design that integrates these two parts into one part, may be used provided it conforms to the guidelines below. Other refinements of the rail system are acceptable if they conform to the following guidelines:-

- An X2 rail must contain all the key attributes of the rail, as defined in this MSA, when assembled IE mounting points, latching features, lead ins, hard stops and guide features etc.
- An X2 rail must provide an equal or greater EMI performance and provide similar pressures on the module during and after insertion relative to the rail defined in this MSA.
- An X2 rail must be useable with all heights of module and not impede air-flow in any direction over the top of the module for all module heights.
- An X2 rail must provide an equal or reduced impedance thermal path from the module to the Host PCB relative to the rail defined in this MSA.
- An X2 rail must provide an equal or greater mechanical stiffness in all respects relative to the rail defined in this MSA.

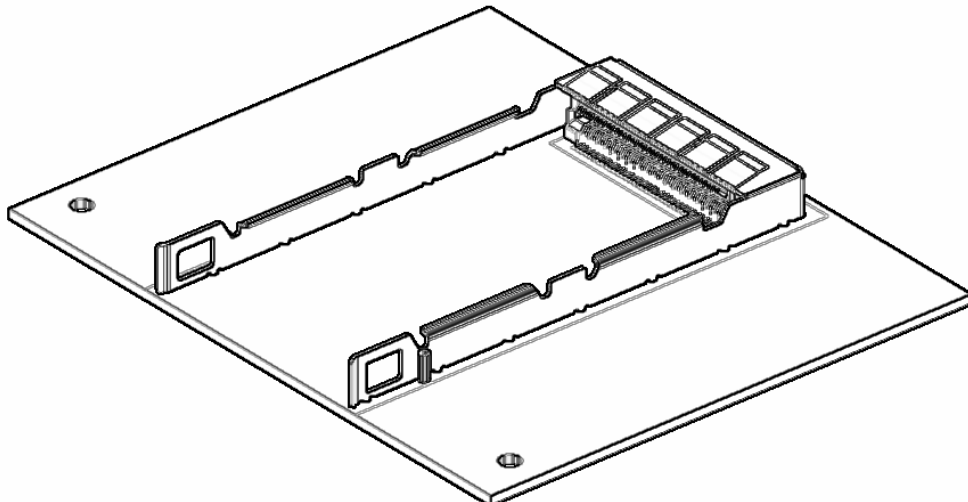
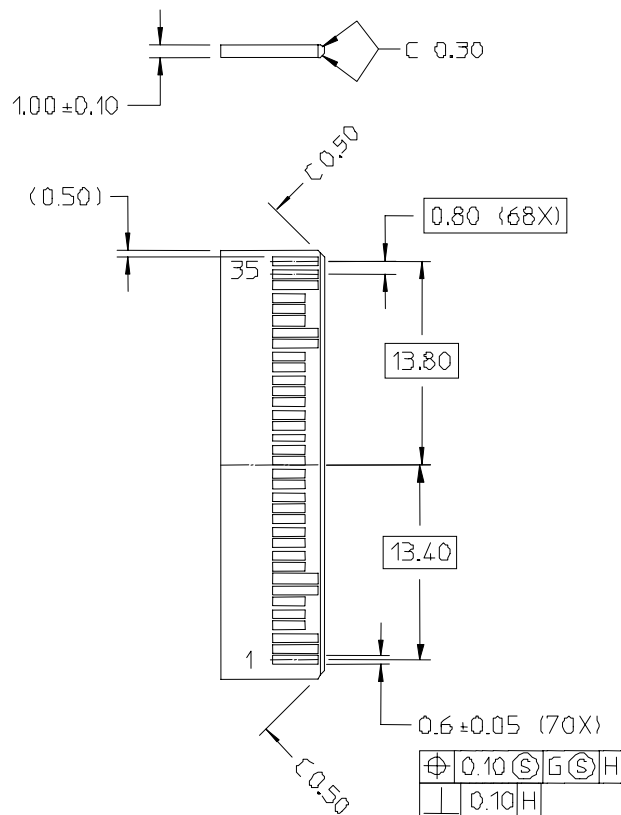
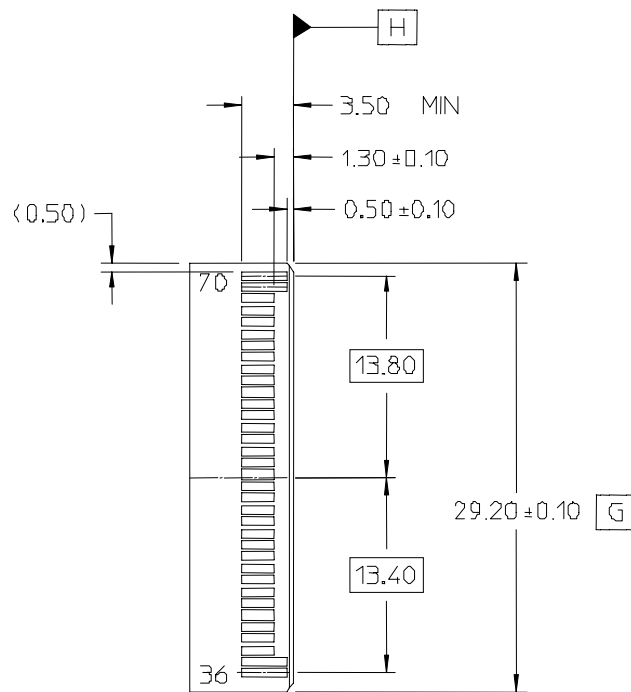


FIG 8. THRU BEZEL RAIL, NOT RECOMMENDED FOR MID-BOARD APPLICATION

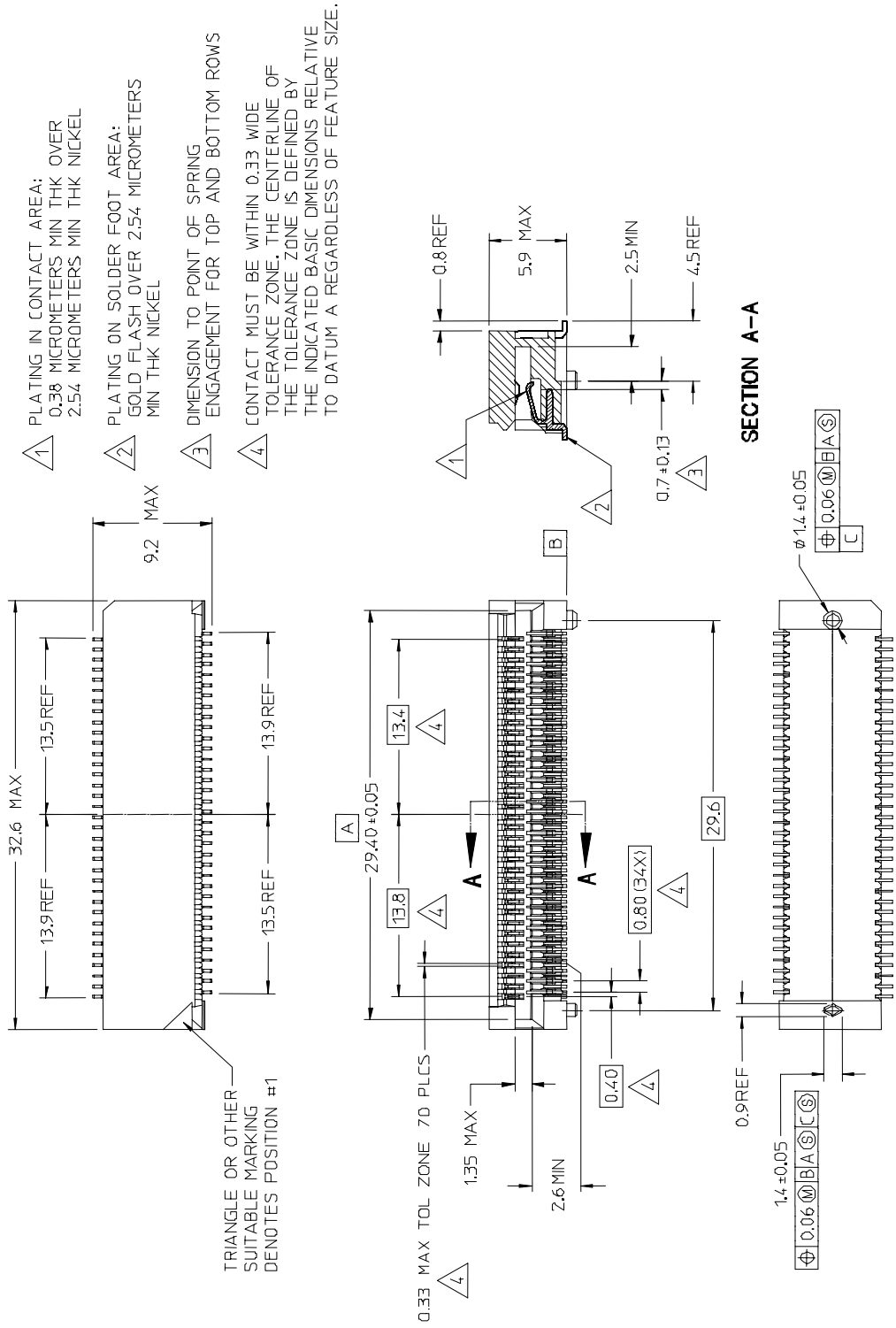
6.5 Datum Definitions

DATUM	DESCRIPTION TRANSCEIVER / LINECARD
<i>A</i>	<i>CUSTOMERS PCB TOP SURFACE</i>
<i>B</i>	<i>PHYSICAL HARD-STOP ON TRANSCEIVER</i>
<i>C</i>	<i>WIDTH OF TRANSCEIVER</i>
<i>D</i>	<i>VERTICAL CENTER OF TRANSCEIVER PCB</i>
<i>E</i>	<i>TOP SURFACE OF RAIL SLOT ON TRANSCEIVER</i>
<i>F</i>	<i>FRONT SURFACE OF CUSTOMERS FACEPLATE</i>
<i>G</i>	<i>WIDTH OF TRANSCEIVER PCB</i>
<i>H</i>	<i>LEADING EDGE OF TRANSCEIVER PCB</i>
<i>J</i>	<i>INSIDE EDGE OF MOUNTING TABS ON RAIL</i>
<i>K</i>	<i>PHYSICAL HARD STOP ON RAIL</i>
<i>L</i>	<i>CENTER OF CONNECTOR LOCATION POINT ON CUSTOMER'S PCB</i>
<i>M</i>	<i>BOTTOM OF RAIL</i>
<i>N</i>	<i>CENTER HOLE LOCATING REAR RAIL ON CUSTOMERS PCB</i>
<i>P</i>	<i>WIDTH OF INSIDE EDGE OF CUT-OUT IN CUSTOMER'S FACEPLATE</i>
<i>R</i>	<i>TOP EDGE OF MOUNTING TABS ON RAIL</i>

6.6 X2 Transceiver PCB Detail.



6.7 X2 70 Pin Electrical Connector.



6.8 X2 70 Module Transceiver.

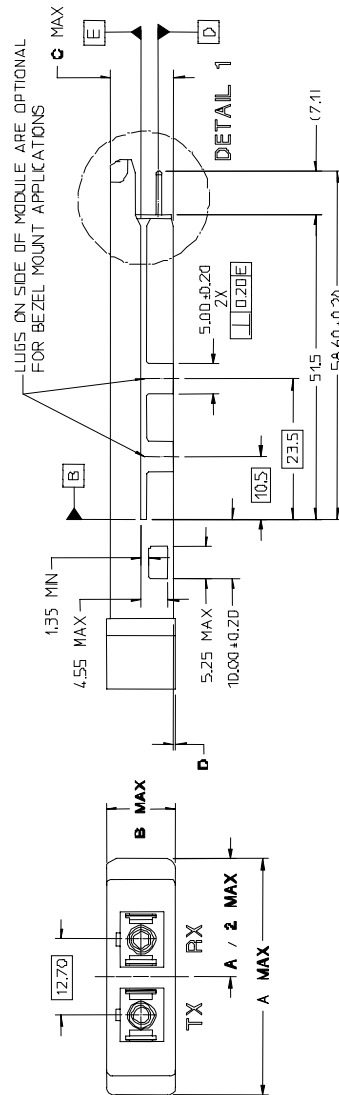
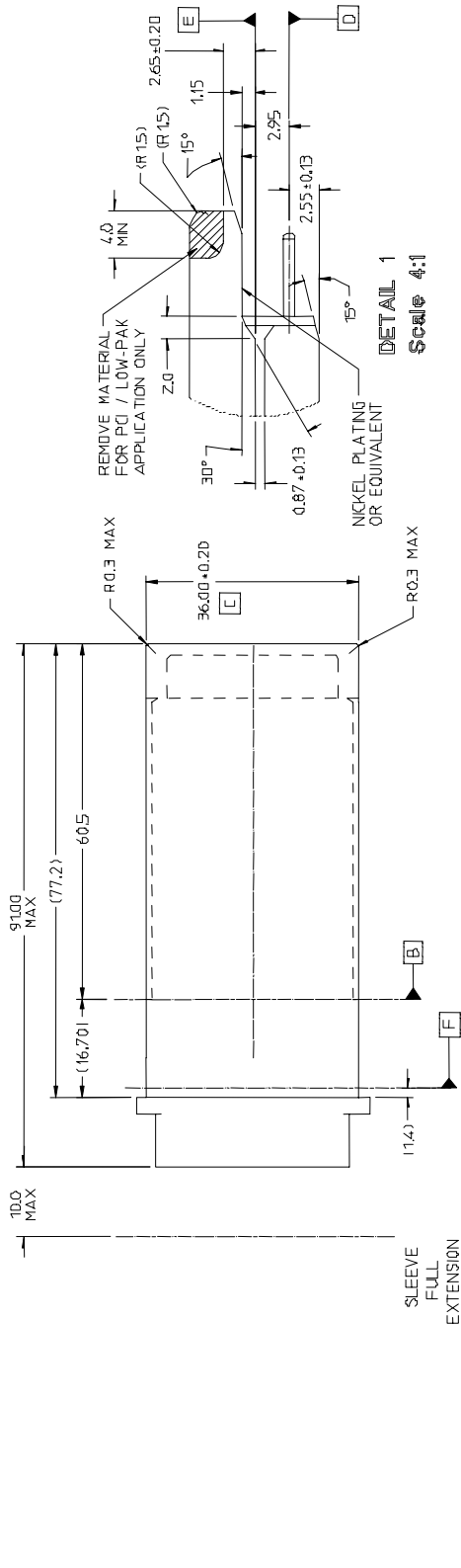


TABLE 1. MODULE VARIANTS

	FC/Low	MIDPAK	HIPAK	MID BOARD
A	42.00	42.00	42.00	EITHER
B	12.00	79.46	28.86	EITHER
C	11.00	13.46	22.86	EITHER
D	0.314/-0.13	3.00 MAX	3.00 MAX	0.314/-0.13

DO NOT SCALE THIS DRAWING	DATE	DESIGN	REVISION
MFG	08/11/09	1.0	1.0
DESIGNER	DATE	DESIGN	REVISION
UNLESS OTHERWISE SPECIFIED	UNLESS OTHERWISE SPECIFIED	UNLESS OTHERWISE SPECIFIED	UNLESS OTHERWISE SPECIFIED
* THIRD ANGLE PROJECTION			

TOLERANCES

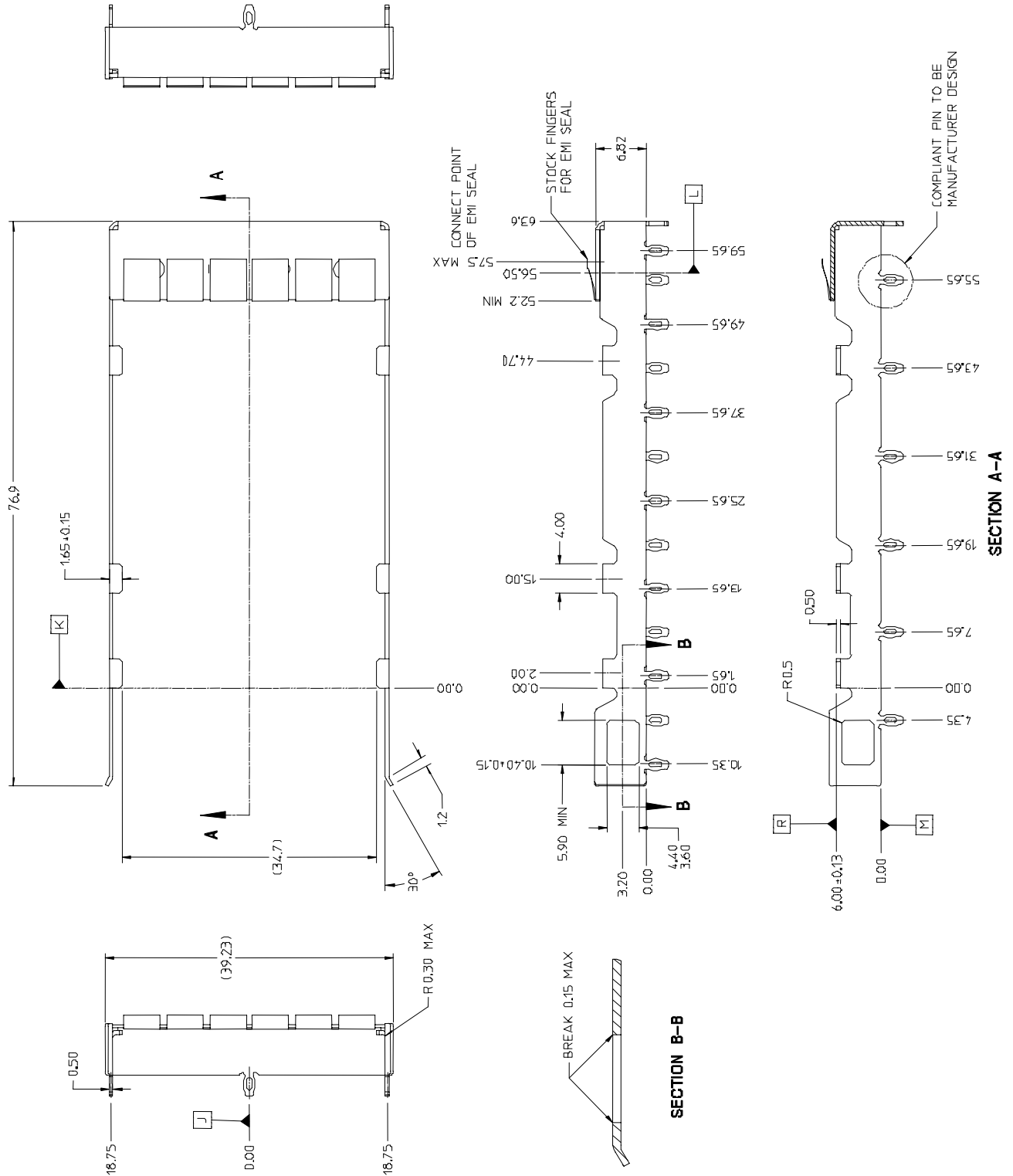
XX ±0.8 mm

XXX ±0.2 mm

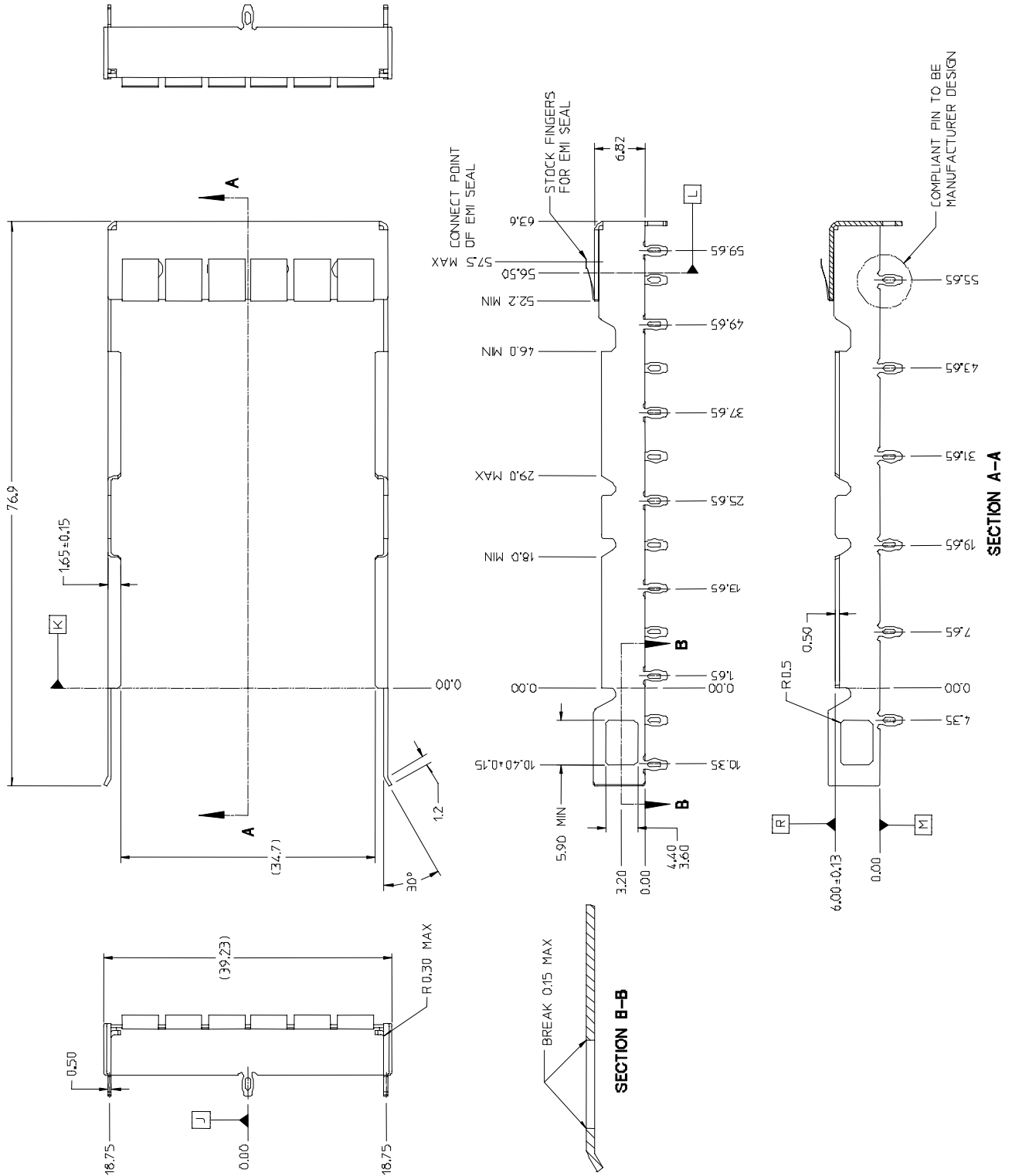
XXXX ±0.1 mm

ALL ±XX.XX mm

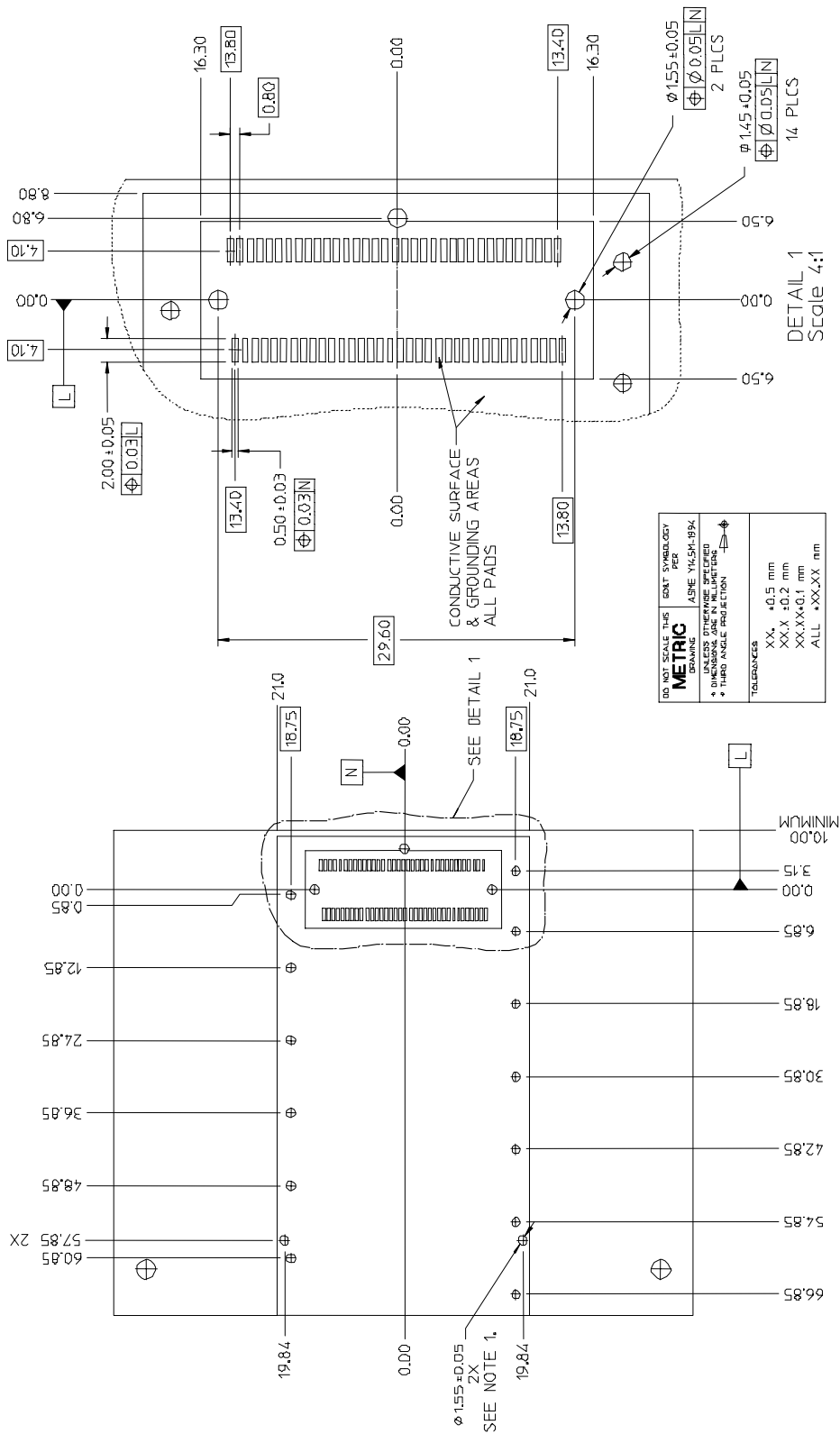
6.9 X2 Mid-Board Mount Rail (Recommended for PCI / LO PAK & Mid Board Application).



6.10 X2 Thru Bezel Rail (Not recommended for Mid-Board Application).

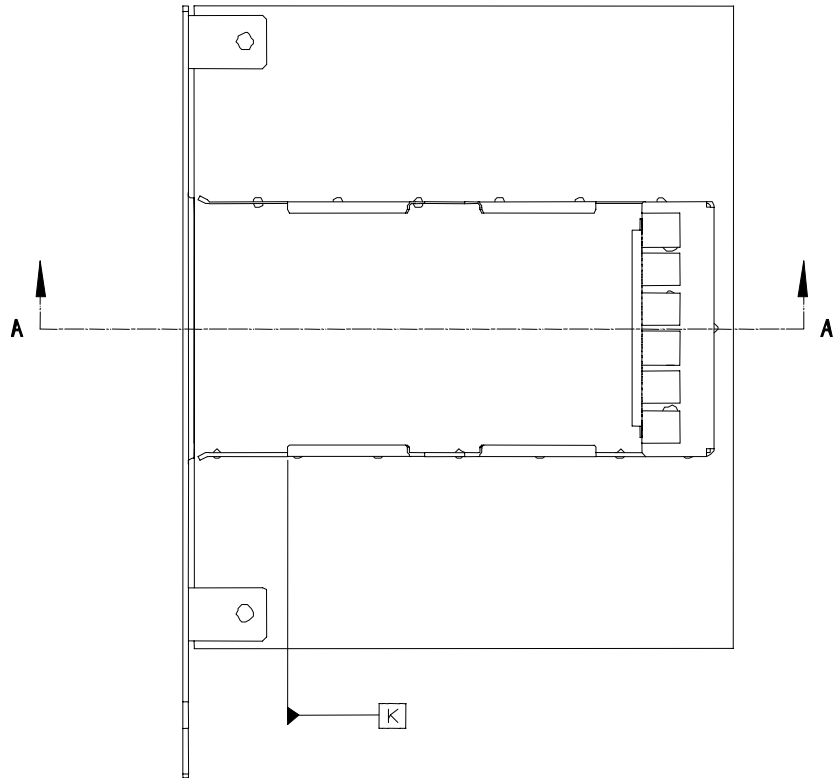
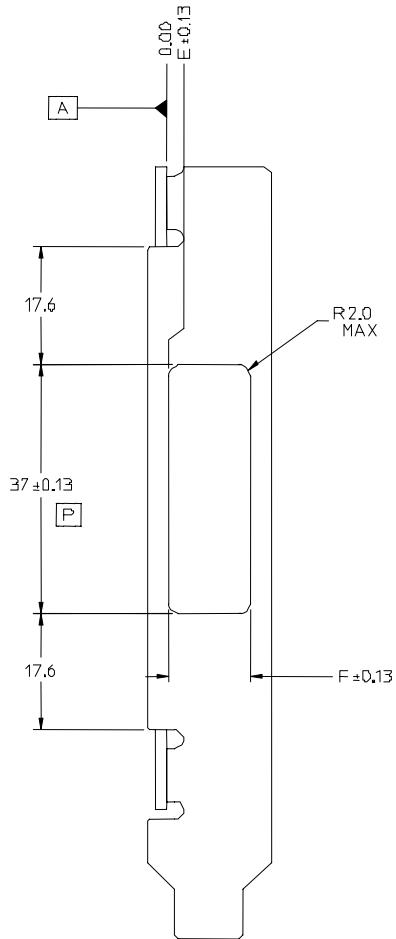


6.11 X2 Host PCB Footprint



NOTES:
 1. OPTIONAL HOLES FOR INCREASING STIFFNESS IN APPLICATIONS WHERE INVERTED MODULES ARE LIKELY. THESE HOLES WOULD CONTAIN STANDARD ROLL PINS, 150mm DIA. LENGTH TO BE DETERMINED BY APPLICATION.

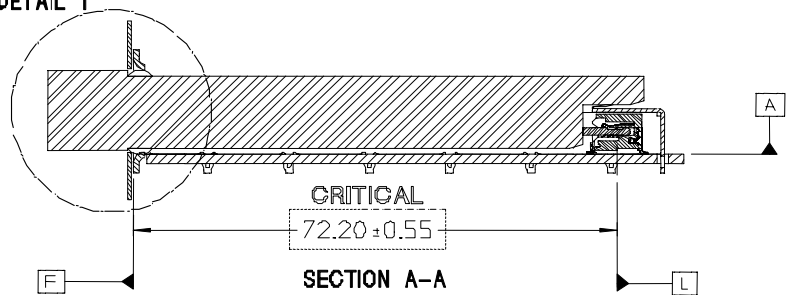
6.12 X2 Conventional PCI Environment.



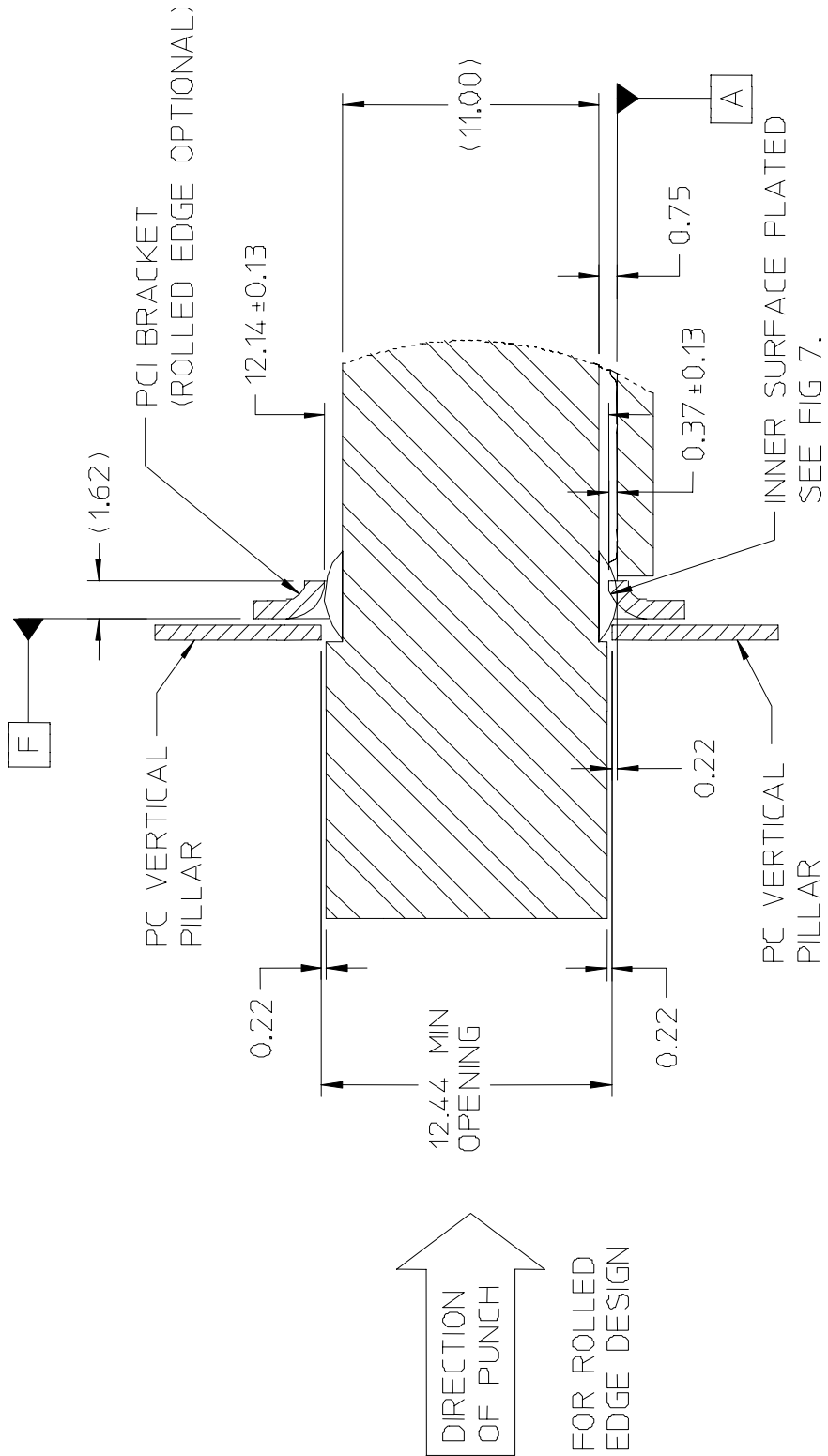
	PCI/LOWPAK	MIDPAK	HIPAK
E	0.37	0.25	0.25
F	12,14	14,46	23,86

NOTE: PCI BRACKET SHOWN

SEE DETAIL 1



6.13 X2 Conventional PCI Environment. (Detail View)



DETAIL 1

6.14 Isometric Drawings of “Conventional” PCI Solution

Note: The following drawings show mounting of a X2 module in a "conventional" 0.47 PCI system as found in traditional computer systems. It is not envisaged that this system will be used for such applications as CPCI that do not impose 12mm width constraint on the face plate and may therefore use a more traditional overlapping "XENPAK style" bezel approach.

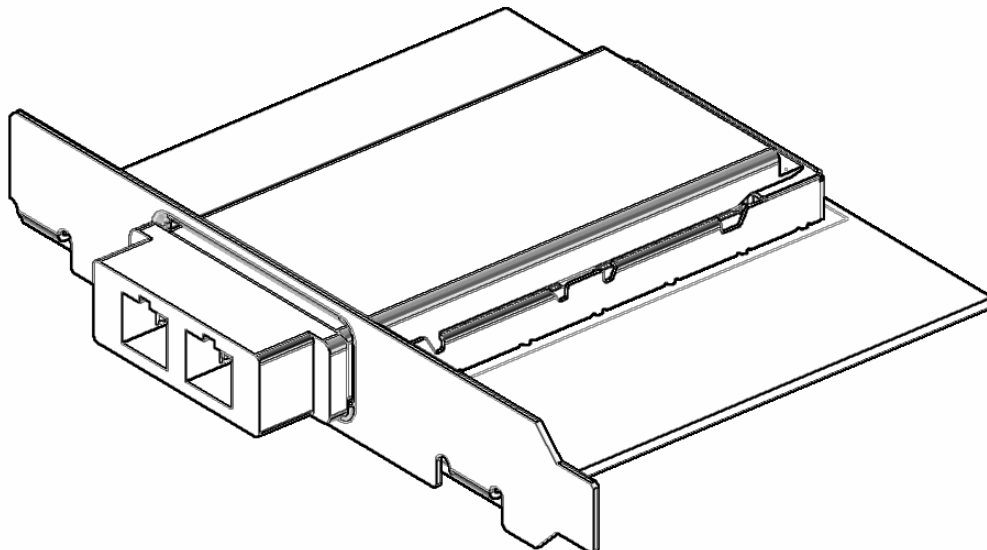


FIG 9. CONVENTIONAL PCI / LOW - PAK

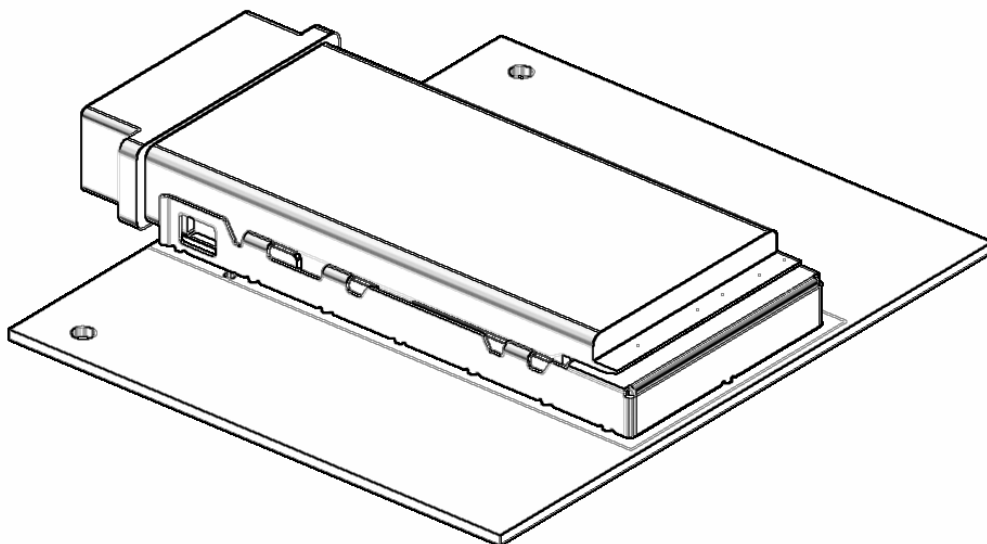


FIG 10. CONVENTIONAL PCI / LOW - PAK

6.15 Isometric Drawings of Front Panel Switch Environment

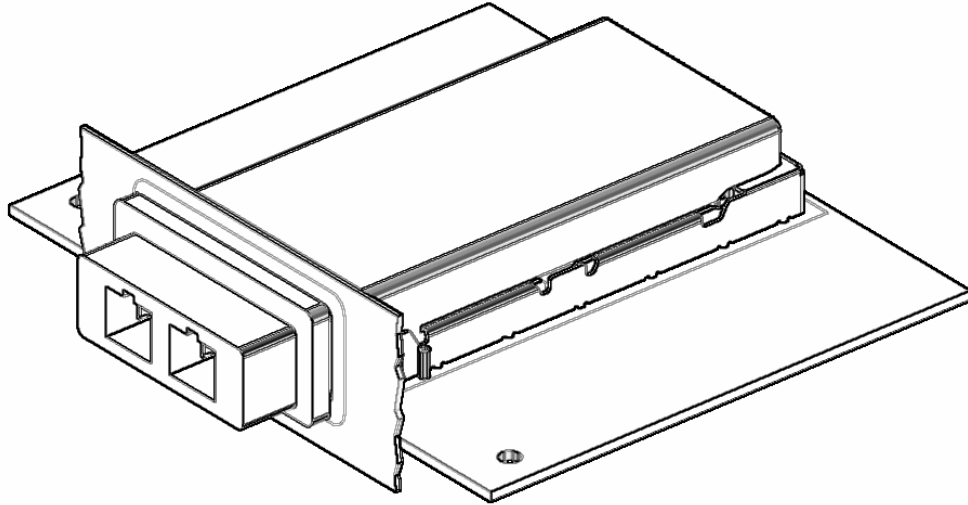


FIG 11. SWITCH PANEL MID / HI - PAK

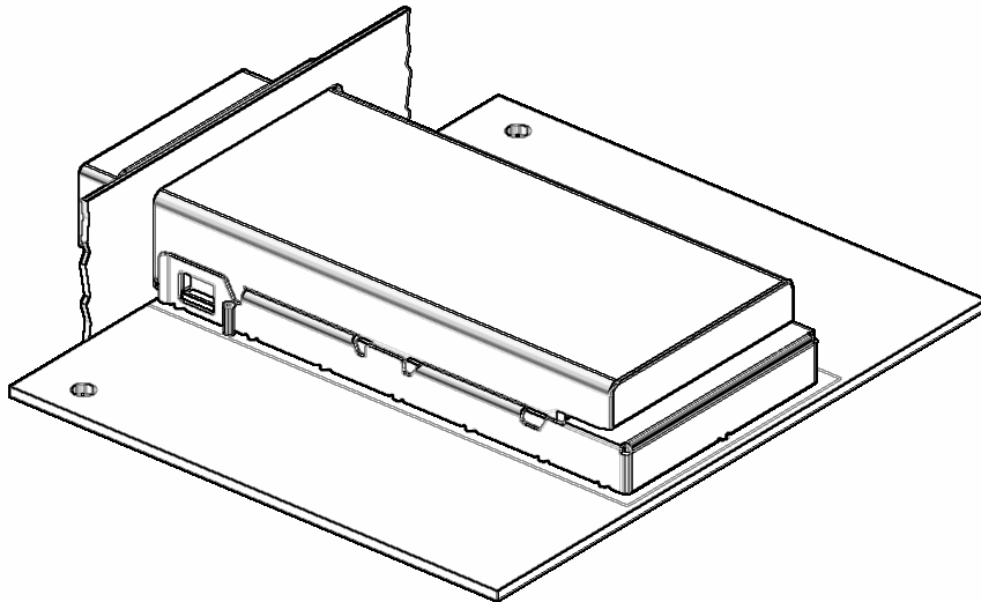
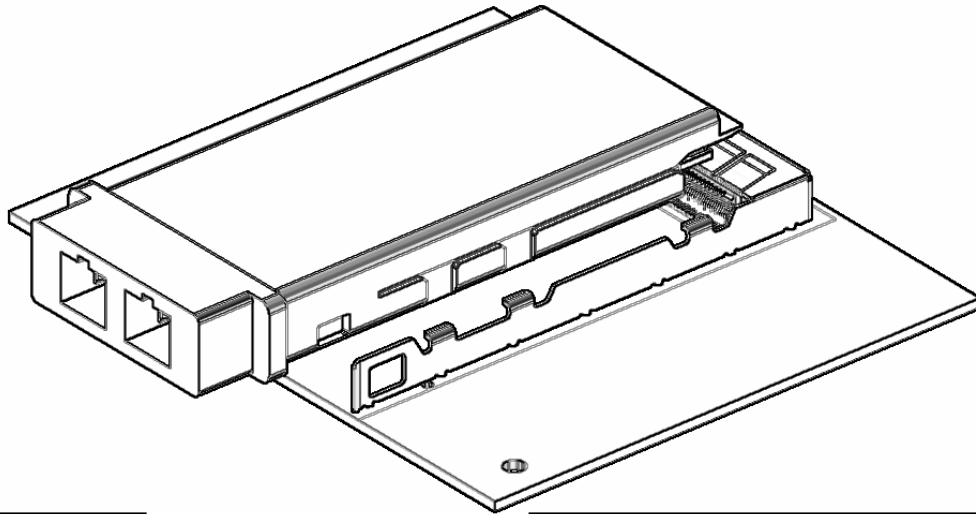


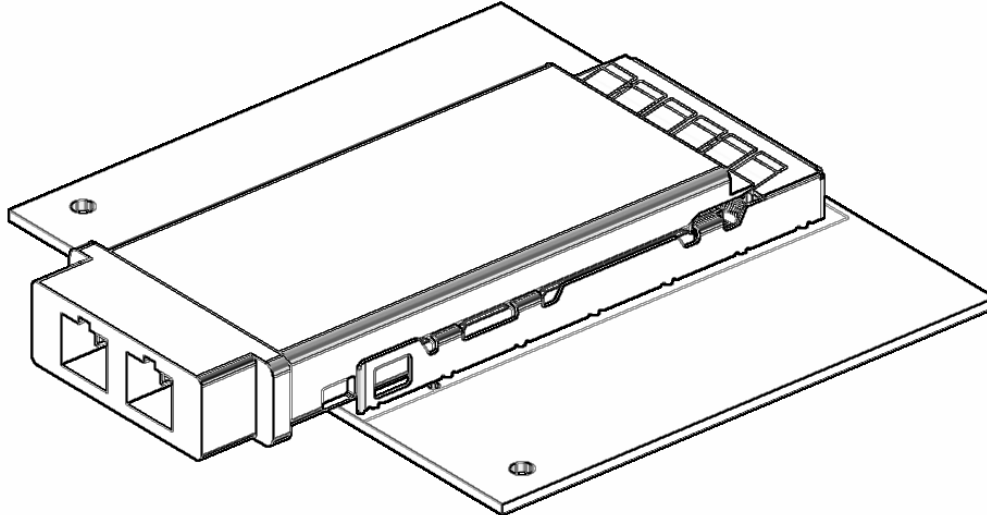
FIG 12. SWITCH PANEL MID / HI - PAK

6.16 Isometric Drawings of Mid-Board Mount Application



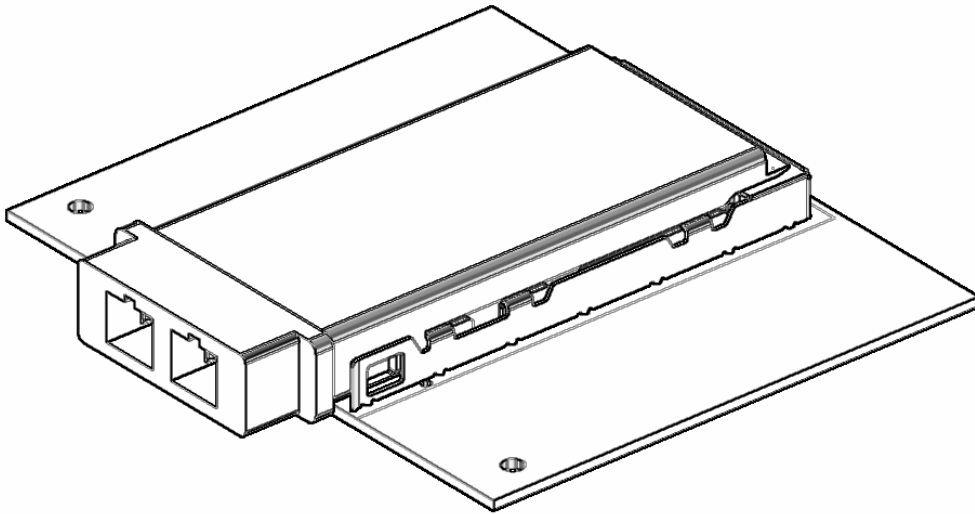
STEP 1.

FIG 13. MID – BOARD MOUNT



STEP 2.

FIG 14. MID - BOARD MOUNT



STEP 3.

FIG 15. MID - BOARD MOUNT

6.17 Optical Interface

The purpose of this section is to specify the optical connector interface sufficiently to insure performance, inter-mateability and supplier flexibility.

6.17.1 Optical Plug

The Optical interface shall use a duplex SC optical plug which conforms to IEC 61754-4. Only the floating duplex style connector plug shall be used. Rigid SC duplex connectors shall not be used. Connector keys are used for transmit/receive polarity.

NOTE: Floating Duplex SC connectors may use two simplex connectors and mechanical coupling to create a single connector that retains both connectors but allows them to “float” within the specified tolerance

6.17.2 Optical Receptacle

The objective of this section is to specify the optical connector interface to sufficiently ensure performance, inter-mateability and maximum supplier flexibility.

6.17.3 Optical Receptacle

The SC Duplex Receptacle shall conform to the requirements of IEC 61754-4 with the following clarification:

The distance between the center line of the active optical bores (ref DB) shall be 12.25/13.15mm to match the floating duplex SC optical plug (ref Duplex optical plug table Note 8).

Increasing this tolerance avoids the restrictive manufacturing tolerance associated with rigid SC connectors.

6.18 Mechanical Forces

The following limits should be observed when designing for, or using X2 transceivers:

Forces are defined for module inserted in correct intended orientation:

- i) Maximum insertion force = 80N
(includes connector, rail and connector shield grounding spring)
- i) Maximum retention force = 50N
- ii) Maximum retention force with latch engaged = 100N



Force defined for module when inserted incorrectly:

- i) Force to insert module when upside down must be >100N

Rail extraction force must be greater than 14.3N per pin.

6.19 Transceiver and Connector Durability

The following life ratings should be observed when designing for, or using, X2 transceivers and their associated connectors:

Minimum mate/de-mate cycles for transceiver = 50 cycles

Minimum mate/de-mate cycles for 70 pin connector = 100 cycles

6.20 PMD Support

This MSA aims to accommodate all XAUI based 10GbE applications.

In order to support multiple interface types the MSA defines 3 different power classes, namely:-

- Class I: up-to 4W maximum power dissipation
- Class II: 4-5W maximum power dissipation
- Class III: >5W maximum power dissipation

The appropriate package style (lo, mid or hi) should be selected depending on the power class of the parts used and the thermal environment of the particular design.

It should be noted that the thermal capacity of X2 is lower than XENPAK.

7. X2 Electrical Interface

The X2 connector is identical to XENPAK, for example TycoAMP Part number 1367337-1, Molex Part No. 74441-0003 or equivalent.

An X2 module will be electrically identical to a XENPAK module apart from the following modifications:-

7.1 X2 Register Set Relative to XENPAK MSA

The X2 register map is identical to XENPAK.

The contents are equivalent to a XENPAK transceiver except:-

- The package OUI, register D.32818 (decimal) D.8032 (hex) is “00-0C-64”, (note this is different from the XENPAK OUI which is 00-08-BE).



- X2 transceiver will use a 00000010 (binary), 0x02 (hex) mask in register d.32786 (decimal) D.8012 (hex) to indicate transceiver type (versus XENPAK which uses 0x01 (hex)).

8. Thermal Verification

The following sections provide recommendations for module vendors and users to model and characterize the thermal behavior of X2 modules. The information is presented for guidance only.

8.1 Assumptions

Maximum case temperature for an X2 module is 70°C. Case temperature is as defined in IEC 60950 section 4.5.1, table 4B.

8.2 Scope

The purpose of this section is to provide guidance to X2 suppliers and users alike to create a consistent test environment. This will identify the limiting boundary conditions to help the efficient thermal system design using X2 modules.

The parameters defined in this section shall enable clear communication of thermal simulation or thermal test data between module supplier and system vendor and will aid correlation between simulation and actual measured results.

This document however does not guarantee system level performance or port density. This will be resolved on a system specific basis.

Any characterization results presented in this thermal section are given as examples only.

8.3 System Design & Assumption for Characterization, Simulations and Measurement

Information presented by the module vendor in relation to this document should be obtained from a “confined or ducted flow” system, as shown in figures 16 and 17.

A blower duct is mounted so that the direction of air flow is parallel to the heat sink fins.

Airflow measurement points are shown in figure 17 as point **X**.

Air flow should be characterized using a calibrated hot wire anemometer placed at the air flow inlet (F1).



Thermocouples should be used to measure case temperature at the worst-case location on a given design.

Each module vendor, as a minimum recommendation, should provide measurement data as recommended in figure 18.

Identical PMD types will be expected to be characterized i.e. no mix of 850nm or 1310nm or 1550nm PMDs is mandated.

When under-going thermal evaluation X2 transceivers should output the idle patterns on both the XAUI and PMD outputs. The idle patterns fro XAUI and PMD are described in IEEE 802.3ae sections 48.2.3.2 and 49.2.4.7 respectively.

Other measurement data provided is at the discretion of the vendor.

8.3.1 Test Environment

The following parameters should generally be recorded during characterization and may be used to de-rated data to standard values:-

- Altitude (sea level)
- Air humidity (50% +/- 10%)
- Inlet Air Temperature (0°C to +50°C)

8.3.2 Variable Parameters

The following parameters may be varied in order to produce the recommended data:-

- Suggested air flows:-

	Minimum	Typical	Maximum
PCI	0.5m/s	1.5m/s	3.5m/s
Switches	1m/s	2m/s	3.0m/s

Air flow will be measured at the pint indicated with an **X** in figure 17 that is within 1cm of both the edge of the card and the front to back mid-point of the module.

- Number of ports: 1 for PCI, 1-8 for switches

8.3.3 Test Fixture

- PCB motherboard must have 4 continuous 2 oz copper layers within.
- The system should provide uniform airflow across the vent opening and be of constant volume air flow
- The MSA specified X2 rail should be used
- A wind tunnel housing with poor thermal conduction will be used – a plastic (IR transparent to allow the potential use of an infra-red camera) is recommended

- Dimensions of system and other features are represented in the drawings documenting the test unit
- For multiple module configurations it is assumed that the conditions drawn for module 1. will be duplicated for module “N”
- Blanking plates will be provided to close the front faceplate when modules are not inserted in the test chamber slots, but they will not fill the slot in the test PCB.
- For multiple module tests the modules will be adjacent to one another with no gaps from empty test chamber slots. It is recommended to fill slots from the slot closest to the inlet and incrementally leeward as modules are added.
- The test chamber will be clear of obstruction for 30cm after the outlet.

8.3.4 Module Conditions

A steady state should be obtained prior to taking measurements.

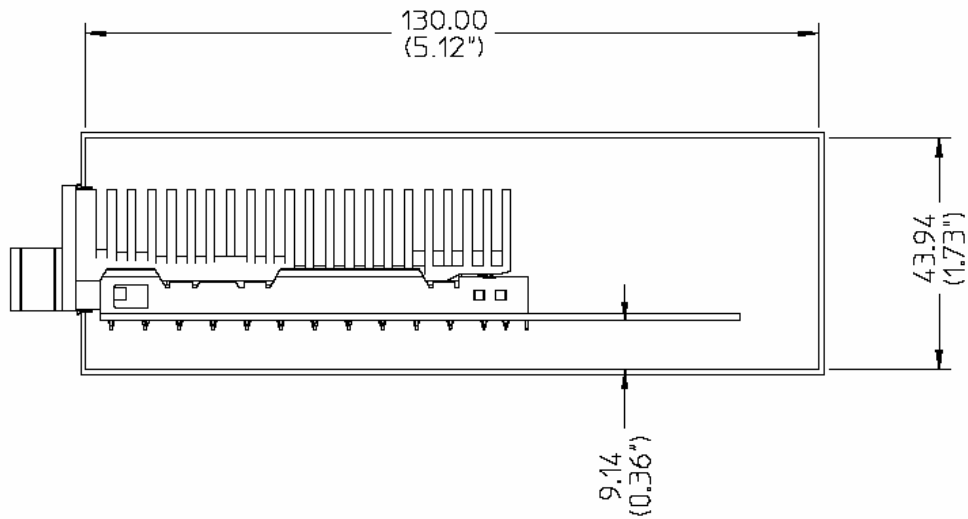


Figure 16 Cross Section of Test Fixture

8.3.5 Temperature Measurement Position

The temperature should be measured at the worst-case location on a module for a given design, when measured under the conditions defined in this section.

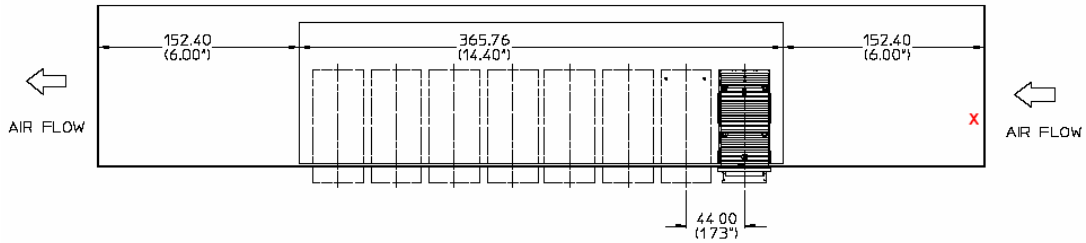


Figure 17 Plan and Side view of Test Fixture

8.3.6 Suggested Data Format

Example data collected according to 8.3.5 will be represented in a chart as described in figure 18.

Case temperature of the hottest module within a multiple or single module configuration will conform to IEC 609950.

Max case temperature conforms to UL1950 under the conditions defined below in the MSA test chamber.

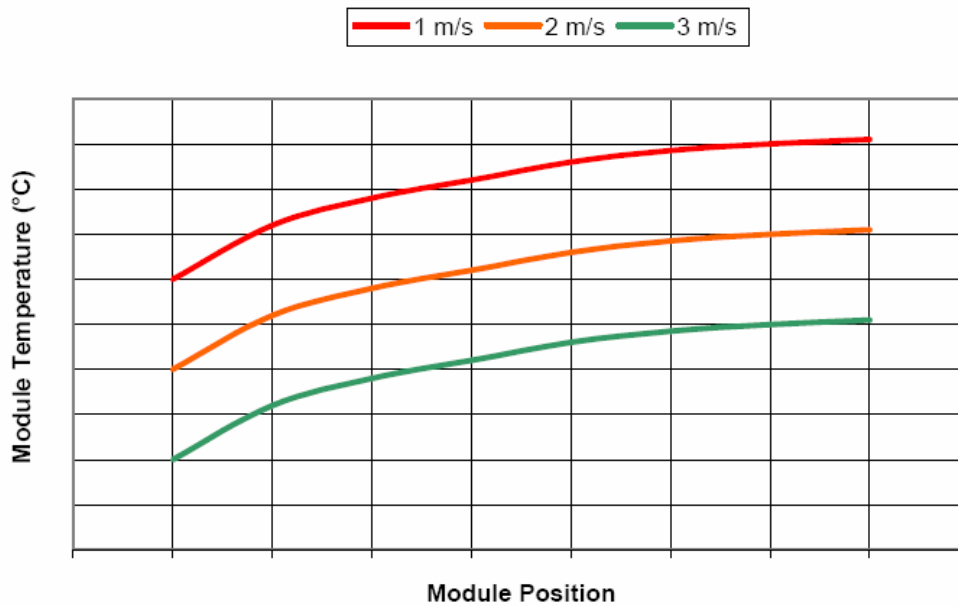


Figure 18 Case temperature vs air inlet temperature and air flow at reference point for a transverse switch

Data should be extrapolated to provide charts relative to 50°C ambient air temperature.



9 Xenpak Errata

This section lists some corrections and clarifications required for the XENPAK MSA revision 3.0 that have been discovered during the development of the X2 MSA. Corrections and clarifications made in this section should not be interpreted as applying retroactively to the XENPAK MSA.

9.1 MDIO interface

The timing requirements of the MDIO electrical interface for a X2 transceiver are defined in IEEE Std 802.3ae-2002 clause 45.4, not clause 45.3 as stated in the notes of Table 11 of the XENPAK MSA revision 3.0. The MDIO electrical interface characteristics are governed by Table 45-65 of IEEE Std 802.3ae-2002. Section 10.5.2 and Table 11 of the XENPAK MSA revision 3.0 should not be interpreted as requiring the MDIO interface to be implemented as open drain connections subject to the electrical characteristics of low speed interface defined in Table 9. If the MDIO interface is implemented using open drain drivers, the host system need not be restricted to the minimum and maximum pull-up resistance values listed in Table 9.