Fundamentals of Bus Differential Protection

Presented by:
Mike Ramlachan
Lead Technical Sales Specialist
Grid Solutions

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Contact Information

Application Engineers

Paul Smith
Paul.J.Smith@ge.com
803-309-9637

Mike Ramlachan
Ravindranauth.ramlachan@ge.com
201-780-6601

Terrence Smith
Terrence.smith@ge.com
423-304-0843

Sales

Eduardo Iglesias
Eduardo.iglesias@ge.com
305-898-6539

Michael McClellan Jr.
McClellan@L-3.com
770-500-9216

John Levine
John@L-3.com
404 626-8312
Today’s Agenda

• Introduction to Bus Protection
• Bus Arrangements and Components
• Protection Techniques
• CT Saturation
• Advanced Algorithm to Handle CT Saturation
Introduction to Bus Protection
Challenges to Bus Zone Protection

High fault current levels can:
• Damage equipment from mechanical stress on busbars
• Lead to CT saturation
• Cause high levels of arc flash

Mal-operation of bus protection has significant impact
• Loss of customer loads may damage customer assets
• Detrimental impact on industrial processes
• System voltage levels stability may be adversely impacted

Bus protection must be dependable and secure, with emphasis on security...
Challenges to Bus Zone Protection

Many different bus topologies
- Switchyard configuration
- Single bus, double bus (single and double breaker), main and transfer bus, breaker-and-a-half and hybrids
- CT placement

Buses may reconfigure at any time
- Different apparatus may be connected/disconnected
- Switching may happen from any number of sources
  - Manually
  - Automatically

Bus protection must adapt automatically (no user intervention) in real-time, based on bus configuration
High-Speed Bus Protection Advantages

Arc flash energy reduction:
- Relay operating times of 12 – 24 ms reduce energy to level 2 in most MV cases
- No impact on system coordination
- Always in operation without operational intervention

Faster return to service following a bus fault:
- Fast operating time minimizes physical damage
- Shorter repair times
Bus Arrangements and Components
Typical Bus Arrangements

Single bus - single breaker

- Distribution and lower transmission voltage levels
- No operating flexibility
- Fault on bus trips all circuit breakers
Typical Bus Arrangements

Multiple bus sections - single breaker with bus tie

- Lower transmission voltages
- Limited operating flexibility
Typical Bus Arrangements

Main and Transfer buses

- Increased operating flexibility
- A bus fault requires tripping all breakers
- Transfer bus for breaker maintenance
**Typical Bus Arrangements**

**Double bus - single breaker with bus tie**

- Very common arrangement at US West Coast substations
- Transmission and distribution voltage levels
- Breaker maintenance without circuit removal
- Fault on a bus disconnects only the circuits connected to that bus
Typical Bus Arrangements

Ring bus

- Higher voltage levels
- High operating flexibility with minimum breakers
- Separate bus protection not required, as the line protections cover overlap bus parts
Typical Bus Arrangements

Breaker-and-a-half bus

- Used on higher voltage levels
- More operating flexibility
- Requires more breakers
- Middle sections covered by the line protection
Protection Techniques
Bus Zone Protection Techniques

All bus zone protections essentially operate based on Kirchoff’s law for currents: “The sum of all currents entering a node must equal zero.”

The only variation is how this is implemented.

Various existing implementations:

• Unrestrained differential
• Interlocking/blocking schemes
• High impedance differential
• Low impedance percent differential
Which Bus Protection Scheme do you specify?

- Unrestrained
- Interlocking/blocking
- High Impedance
- Low Impedance
- None
Unrestrained Differential (Overcurrent)

- Differential current created by physically summing CTs
- CT ratio matching required (auxiliary CTs)
- External faults may cause CT saturation, leading to spurious differential currents
  - Intentional time delay added to cope with CT saturation effects
- Unrestrained differential function useful in microprocessor-based protections (check zone)

Intentional time delay means no fast zone clearance
Interlocking/Blocking Schemes

- Blocking signals generated by downstream protections (usually instantaneous overcurrent)
- Simple instantaneous overcurrent protection with short intentional time delay
  - Need to wait for blocking signals
  - Usually inverse timed backup provided
- Timed backup may be “tricked” by slow clearance of downstream faults.
- Blocking can be done via hardwire or communications (e.g., GSSE/GOOSE, dedicated communications)

Technique limited to radial circuits with negligible backfeed
High Impedance Differential (Overvoltage Typically)

- Operating signal created by connecting all CT secondaries in parallel
  - CTs must all have the same ratio
  - Must have dedicated CTs
- Overvoltage element operates on voltage developed across resistor connected in secondary circuit
  - Requires varistors or AC shorting relays to limit energy during faults
- Accuracy dependent on secondary circuit resistance
  - Usually requires larger CT cables to reduce errors » higher cost

Cannot easily be applied to reconfigurable buses, no advanced functionality (oscillography, breaker fail)
High Impedance Differential Philosophy

- \( i_1 + i_2 + i_3 + \ldots + i_n = 0 \)  
  The vectorial sum of all primary currents in and out of the bus equals zero

- \( i_1 + i_2 + i_3 + \ldots + i_n = 0 \)  
  The vectorial sum of all CT secondary currents (assuming same CT ratio and no CT saturation) in and out of the bus equals zero

- \( v_1 + v_2 + v_3 + \ldots + v_n = 0 \)  
  The vectorial sum of all voltages induced on all CT secondary windings during normal load or external fault (no CT saturation) equals zero

None of the above equations hold true during internal fault or external fault with CT saturation
High Impedance Bus Protection

- Fast, secure and proven. Can be economical
- Can be applied to small or large buses
- Require dedicated CTs, preferably with the same CT ratio. Cannot handle nicely inputs from CTs set on different taps.
- Input from not fully distributed CT winding creates danger for the equipment, because of inducing very high voltages – autotransformer effect
- Depending on bus internal and external fault currents, they may not provide adequate settings for sensitivity and security
- Cannot be easily applied to re-configurable buses
- Require a voltage limiting varistor capable of absorbing significant energy
- Does not provide benefits of a microprocessor based relay (e.g. metering, monitoring, oscillography, breaker fail)
High Impedance Bus Protection (HS O/C + HID)

Comprised of the following:

• **F35 Relay** - high speed overcurrent relay

• **High Impedance Module (HID) with Stabilizing Resistors and Voltage Limiters**
  The F35 relay (high speed overcurrent relay) connected in series with the stabilizing resistors provide high speed operation for bus faults involving high-magnitude currents. A voltage limiting element (MOV) is connected in parallel to avoid excessively high CT secondary voltages that can damage the current inputs when the relay fault occurred.

• **Lockout Relay & Push Button**: Mechanical lockout after relay operation and Reset Button. Four additional normally open contacts available for use.
High Impedance Bus Protection (F35 + HID)

Output of parallel CTs

F35 Relay

- High Speed Overcurrent Module
- Use Phase IOC element of F35 relay to operate 86 TRIP and RELAY TRIP
- Reset via HID reset button or use F35 contact input to control an output on 86

86 RESET CAN BE ACHIEVED:
- VIA THE RESET PUSHBUTTON
- WIRING A RELAY OUTPUT

Multilin HID
High Impedance Differential Module
Model HID32 or HID31

To external 86 Lockout Relay that trips each breaker
Low Impedance Differential

- **Percent** characteristic used to cope with CT saturation
- **Restraining** signal can be formed in a number of ways
- No dedicated CTs needed
- Protection of re-configurable buses possible

\[
I_{DIF} = |I_1 + I_2 + \ldots + I_n| \\
I_{RES} = |I_1| + |I_2| + \ldots + |I_n| \\
I_{RES} = \max(|I_1|, |I_2|, \ldots, |I_n|)
\]
Low Impedance (Percent) Differential

- Differential signal formed by summation of the bus currents
- CT ratio matching may be required
- On external faults saturated CTs yield spurious differential current
- Time delay used to cope with CT saturation
- Instantaneous (unrestrained) differential OC function useful on integrated microprocessor based relays
Low Impedance (Percent) Differential

- No need for dedicated CTs
- Internal CT ratio compensation 32:1
- Advanced algorithms supplement percent differential protection function making relay secure
  - CT saturation detection
  - Dual protection principle
- Protection of re-configurable busbars becomes easy as the dynamic bus replica (bus image) can be accomplished without switching physically secondary current circuits
- Integrated breaker fail (BF) function can provide optimal tripping strategy depending on the actual configuration of a busbar
- Distributed architectures replace CT wires with fiber
B30 Protection Low Impedance (up to 6 circuits)

- **MAIN PROTECTION**
  - Two Bus Differential (87B) zones:
    - Restrained and Unrestrained (instantaneous)
    - Dynamic Bus Replica

- **OTHER**
  - Breaker Failure per breaker
  - CT Trouble (50/74)
  - FlexElements™
B90 Low Impedance Bus Protection

- Up to 24 circuits in a single zone without voltage supervision
- Multi-IED architecture with each IED built on modular hardware (single to multiple chassis)
- Up to 96 digital inputs per B90 IED
- Up to 48 output contacts per B90 IED
- Flexible allocation of AC inputs, digital inputs and output contacts between the B90 IEDs

[24 Circuit Applications]
B30/B90/B95 Low Impedance Bus Protection

• Excellent performance:
  ▪ Typical response time: 12 msec + output contact
  ▪ Maximum response time: 16 msec + output contact
  ▪ Very good stability on external faults

• Straight forward to configure
Protecting Re-configurable Buses
Protecting Re-configurable Buses
Protecting Re-configurable Buses
Protecting Re-configurable Buses
Digital Differential Algorithm Goals

• Improve the main differential algorithm operation
  – Better filtering
  – Faster response
  – Better restraint techniques
  – Switching transient blocking

• Provide dynamic bus replica for reconfigurable busbars

• Dependably detect CT saturation in a fast and reliable manner, especially for external faults

• Apply additional security to the main differential algorithm to prevent incorrect operation
  – External faults with CT saturation
  – CT secondary circuit trouble (e.g. short circuits)
POLL #2

Would like us to contact you to help you design and/or upgrade your bus differential protection or answer any questions you might have?

1. Yes
2. No
CT Saturation
CT Saturation – External Fault with Ideal CTs

- Fault starts at $t_0$
- Steady-state fault conditions occur at $t_1$

Ideal CTs have no saturation or mismatch thus produce no differential current
CT Saturation – External Fault with CT Saturation

- Fault starts at $t_0$, CT begins to saturate at $t_1$
- CT fully saturated at $t_2$

$\begin{align*}
\text{t0} & \quad \text{– fault inception} \\
\text{t1} & \quad \text{– CT saturation time} \\
\text{t2} & \quad \text{– CT saturated}
\end{align*}$

CT saturation causes increasing differential current that may enter differential element operate region.
Some Methods of Securing Bus Differential

• Block the bus differential for a period of time (intentional delay)
  – Increases security as bus zone will not trip when CT saturation is present
  – Prevents high-speed clearance for internal faults with CT saturation or evolving faults

• Change settings of the percent differential characteristic (usually Slope 2)
  – Improves security of differential element by increasing the amount of spurious differential current needed to incorrectly trip
  – Difficult to explicitly develop settings (Is 60% slope enough? Should it be 75%?)

• Apply directional (phase comparison) supervision
  – Improves security by requiring all currents flow into the bus zone before asserting the differential element
  – Easy to implement and test
  – Stable even under severe CT saturation during external faults
Typical Bus Differential Settings
Advanced Algorithm to Handle CT Saturation
Advanced Algorithm of 87B Function

- Large currents
- Quick saturation possible due to large magnitude
- Saturation easier to detect
- Security required only if saturation detected
- Low currents
- Saturation possible due to dc offset
- Saturation very difficult to detect
- More security required
87B Bus Differential Protection

Protection logic

Directional flag

Saturation flag
87B Bus Differential Protection

(DIF₂ = 1 & SAT = 1) Check directional flag! DIR = ?

(DIF₂ = 1)

SAT = 1

OPERATE

BLOCK

|I_D|

Differential current

I_R

Restraining current

LOW SLOPE

HIGH SLOPE

PICKUP

LOW BPNT

HIGH BPNT

1 2 3 4 5 6

1 2 3 4

SAT = 1 (DIF₁ = 1 & SAT = 1)
87B Bus Differential Protection

Protection logic

- \( DIF_1 \)
- \( DIR \)
- \( SAT \)
- \( DIF_2 \)

\[ DIF = \text{AND} (DIF_1 \text{ OR } DIF_2) \text{ AND } \text{SAT} \]

\[ \text{TRIP} = \text{OR} (DIF \text{ OR } \text{DIR}) \]

Directional flag

\( \text{DIR} = 1 \)

Saturation flag

\( \text{SAT} = 0 \)

INTERNAL FAULT

CB 1
CB 2
CB 3
CB 4
CB n
87B Bus Differential Protection

- Differential current $|I_D|$
- Restraining current $I_R$
- LOW BPNT
- HIGH BPNT
- LOW SLOPE
- HIGH SLOPE
- OPERATE
- BLOCK

- $DIF_1 = 1$
- $DIR = 1$

Diagram shows the relationship between differential current and restraining current, highlighting various operating and blocking zones.
87B Bus Differential Protection

(DIF₂ = 1 & SAT = 0) Don’t check directional flag!

High BPNT

Low BPNT

Operate

Block

PICKUP

|D| I |

High Slope

Low Slope
Conclusion

• Dual slope, dual breakpoint characteristic with smooth transition between the slopes
• CT saturation detection
• Dual protection principle
• Typical response time: 12 msec + output contact
• Maximum response time: 16 msec + output contact
• Stability on external fault